VILNIUS UNIVERSITY
SEMICONDUCTOR PHYSICS INSTITUTE

Dainius Šalucha

PASSIVATION OF THE *p-n* JUNCTION EDGE IN HIGH-POWER SEMICONDUCTOR SILICON DEVICES

Summary of Doctoral Dissertation

Technological Sciences, Material Engineering (08T)

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The investigations have been carried out at Vilnius University and Semiconductor Physics Institute in 2004 to 2009.

Scientific Supervisor:
Dr. Sci. Irena Šimkienė (Semiconductor Physics Institute, Technological Sciences, Material Engineering - 08T)

Defence of Dissertation will be held at Council of Materials Engineering Science trend:

Chairman
Prof. Dr. Sci. Steponas Ašmontas (Institute of Semiconductor Physics, Technological Sciences, Material Engineering - 08T)
Members
Prof. Dr. Sci. Antanas Feliksas Orliukas (Vilnius University, Technological Sciences, Material Engineering - 08T)
Prof. Dr. Sci. Sigitas Tamulevičius (Kaunas University of Technology, Technological Sciences, Material Engineering - 08T)
Assoc. Prof. Dr. Bonifacas Vengalis (Institute of Semiconductor Physics, Technological Sciences, Material Engineering - 08T)
Prof. Dr. Sci. Rimas Vaišnoras (Vilnius Pedagogical University, Physics Science, Physics – 02P)

Opponents:
Prof. Dr. Sci. Albertas Laurinavičius (Semiconductor Physics Institute, Technological Sciences, Material Engineering - 08T)
Prof. Dr. Sci. Kęstutis Juodkazis (Institute of Chemistry, Physics Science, Chemistry – 03P)

Public defence of the Dissertation will take place at the open meeting in the in Conference Hall of Semiconductor Physics Institute at 10 a.m. on June 19, 2009.
Address: A. Goštauto str.11, LT-01108 Vilnius, Lithuania.
Tel. (8-5) 261 97 59, fax (8-5) 262 71 23; e-mail spiadm@pfi.lt
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VILNIAUS UNIVERSITETAS
PUSLAIDININKIŲ FIZIKOS INSTITUTAS

Dainius Šalucha

DIDELĖS GALIOS PUSLAIDININKINIŲ SILICIO PRIETAISŲ *p-n* SANDŪROS KRAŠTO PASYVACIJA

Daktaro disertacijos santrauka

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Mokslinis vadovas:
Doc. habil. dr. Irena Šimkienė (Puslaidininkių fizikos institutas, technologijų mokslai, medžiagų inžinerija – 08T)

Disertacija ginama Puslaidininkių fizikos instituto medžiagų inžinerijos mokslo krypties taryboje:

Pirmininkas
Prof. habil. dr. Steponas Ašmontas (Puslaidininkių fizikos institutas, technologijos mokslai, medžiagų inžinerija – 08T)
Nariai:
Prof. habil. dr. Antanas Feliksas Orliukas (Vilniaus universitetas, technologijų mokslai, medžiagų inžinerija – 08T)
Prof. habil. dr. Sigitas Tamulevičius (Kauno technologijos universitetas, technologijų mokslai, medžiagų inžinerija – 08T)
Doc. dr. Bonifacas Vengalis (Puslaidininkių fizikos institutas, technologijų mokslai, medžiagų inžinerija – 08T)
Prof. habil. dr. Rimas Vaišnoras (Vilniaus pedagoginis universitetas, fiziniai mokslai, fizika – 02P)

Oponentai:
Prof. habil. dr. Albertas Laurinavičius (Puslaidininkių fizikos institutas, technologijų mokslai, medžiagų inžinerija – 08T)
Prof. habil. dr. Kęstutis Juodkazis (Chemijos institutas, fiziniai mokslai, chemija – 03P)

Disertacija ginama viešame Puslaidininkių fizikos instituto tarybos posėdyje 2009 m. birželio 19 d., 10 val. posėdžių salėje.
Adresas: A. Goštauto g. 11, LT-01108 Vilnius, Lietuva.
Tel. (8-5) 261 97 59, faksas (8-5) 262 71 23; el. paštas spiadm@pfi.lt
Disertacijos santrauka išsiųsta 2009 m. gegužės 19 d.

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Introduction

Modern high-power semiconductor devices covering a wide range of frequency and power have found application in many areas such as high voltage transmission systems, control of power motors, automotive electronics and switch mode power suppliers in lighting systems, etc. These devices are perspective to handle the high voltages and currents at high speed though at present there are no solutions to satisfy these requirements simultaneously. The main difficulty appears when matching the static parameters of device, such as leakage current and breakdown/on-state voltage, with dynamic functions, such as reverse recovery duration and recovery softness of power switches. Static parameters are limited by the operational range for breakdown voltage and heat dissipation. Dynamic parameters are determined by the necessary switching frequency and limitations for inductive currents induced by active device over external circuits. Carrier transport and generation/recombination parameters of material used in the device design and technology determine the static and dynamic characteristics mentioned above. The trade-off in design of the structure and material physical parameters should also be reached when selecting the device type, the junction type, the doping level and profile, the recombination defects, etc. Therefore, a lot of problems in material science and technology should be solved to optimize the characteristics of the state-of–the-art industrial implementations in fabrication of high-power semiconductor devices.

Thin dielectric passivation layer is one of the basic construction elements in semiconductor device technology. There are few materials, from which the layers may be manufactured. They are oxides mainly, with $Si0_2$ as the most popular of them, although, the phosphor- and boron-silicon glasses are used as passivation layers, too. In choosing a passivant of power thyristors and diodes, there are two important considerations in addition to the usual requirement for providing uniform high breakdown voltage via substrate. One consideration is the thermal stability of the passivant to subsequent high-temperature processes. The other consideration is the bias-temperature stability of the passivation layers affecting the operation life expectancy of a device. In the technology of thyristors and diodes on silicon substrates the bias-breakdown voltage is not uniform over substrate due to non-homogeneity of passivated surface of the p-n junction.

Recently, a large interest in application of porous silicon layers has arisen as the result of new demands as well as new possibilities given by a great progress in IC planar technology. The most widely applied features of porous silicon for solar cell applications include antireflection coating, surface texturing and surface passivation. Porous silicon can be also applied in the technology of high power silicon devices. In this work a new passivation scheme is proposed which is based on a formation of nanostructured layer for passivation of the surface of space charge region. This work is focused on the development of a simple technique for a rapid formation of porous silicon layer as a passivation coating for typical crystalline silicon industrial power thyristors and diode structures.

Beveled-edge termination of the junctions by selectively etched moats is one of the basic technology types to increase a breakdown voltage and switching rates of the commercial power devices. The passivation of junction surface within etched grooves is crucial for providing the device hardiness with respect to high surface electric fields.

The surface charge controlled by passivants is also important in suppressing the leakage currents, caused by surface recombination, and in regulation of electric fields within the bulk of devices. Therefore, in order to increase the stability of a junction, different passivation techniques are being designed and exploited along with commonly used rubberized coatings. Control of surface passivation characteristics is also an important issue for improvement of junction isolation technology.

In this work, passivation of moat surface by means of electrochemical etching, formation of hydrogen-rich porous silicon layers and glass in-melting steps has been investigated. Passivation quality was controlled by the measurements of surface recombination characteristics after each technological step using a non-invasive technique, which employed microwave probed photoconductivity transients (MW-PCT). It has been shown that electrochemical etching - glass melting steps involved in passivation technological procedures resulted in a decrease of surface recombination velocity from $3\cdot10^3$ cm/s to 10 cm/s. Thus, the passivation quality approached to that of suppressed surface recombination velocity obtained for silicon wafers exploiting the iodine ethanol solutions.

The tasks of this work:

- to investigate the regularities in wet chemical etching of isolation grooves; to determine the dependence of parameters of isolation grooves on the composition and temperature of etching mixture, etching device construction and operation principle;
- to investigate the temperature profiles of SiO_2-PbO-Al_2O_3-B_2O_3 glass melting process by means of developed and installed in production line the monitoring system for diffusion furnace. To determine and optimize the dependence of thyristor electric parameters on the temperature regime at filling the isolation grooves with glass;
- to study the application possibilities of diamond like carbon (DLC) coating in the passivation technology of high power semiconductor devices. To investigate the composition and structure of DLC and estimate the passivation quality of p-n junctions;
- to investigate surface recombination regularities in the grooves of thyristor and diode structures under various surface treatments;
- to study the application of porous silicon in the passivation technology of high power devices.
- to investigate the homogeneity mapping of Si wafers by millimeter waves in order to reveal the changes after the main steps of technological procedures.

Scientific novelty and practical significance

1. The regularities of chemical etching of isolation grooves in the formation of thyristor and diode discreet elements have been investigated. Basing on the results obtained, the optimal technology for the formation of isolation grooves was developed and new-construction device for selective chemical etching of semiconductor structure was installed in “Vilnius Venta Puslaidininkiai”, Ltd.
2. In cooperation with “Melrada”, Ltd., the monitoring system of temperature and

gas-composition parameters in glass-passivation diffusion furnace was developed and installed in “Vilnius Venta Puslaidininkiai”, Ltd. Time-dependent temperature profile of SiO_2-PbO-Al_2O_3-B_2O_3 glass melting process was firstly determined and analyzed.

3. The DLC *a*:C-H coatings were shown to passivate efficiently the p-n junctions of high-power semiconductor devices. Basing on these results, the high-power high-voltage (4 kV) gate turn off (GTO) thyristor was developed.
4. Studies of carrier recombination in thyristor and diode structures produced by “Vilnius Venta Puslaidininkiai”, Ltd., allowed us to estimate the efficiency of p-n junction passivation and optimize the passivation process by using porous silicon.
5. The millimeter-waves technique was firstly applied for investigations of homogeneity of Si wafers used in “Vilnius Venta Puslaidininkiai”, Ltd. This technique was determined to be adjusted for control of homogeneity in initial wafers and after diffusion process, *i.e.*, at primary technological steps.

Statements to be defended:

1. Isolation groove with smooth p-n junction surface is optimally formed using etching mixture HF : HNO_3 : CH_3COOH (1.7 : 3.35 : 2.0), the selectivity of which is 106. Established technology is used in a new device construction, in which the etching cell rate and removal of etching mixture from the surface of wafers are controlled.
2. In thyristor structures, the breakedown voltage is caused by isolation groove depth and glass adhesion. The optimal depth of grooves is determined to be 104 μm and the best adhesion of SiO_2-PbO-Al_2O_3-B_2O_3 glass is achieved at melting the glass at 760°C in the constant temperature zone in N_2+O_2 ambient.
3. As followed from the passivation studies of p-n junctions by investigations of carrier surface recombination, in thyristor structures the breakdown voltage depends on the packing defects in highly-doped regions of p-n junctions and high (up to 10^{17} cm^{-3}) residual concentrations of metal ions, which have been formed during standard technological procedures. In new technology, the concentration of packing defects and residual metal ions are significantly reduced due to gettering in electrochemically formed porous Si layer that is removed before glass passivation. The proposed technology ensures an increase of yield by 8% in industrial production of high power Si devices.

Brief Summary of Dissertation

The dissertation is composed of an introduction and three chapters. The manuscript (132 pages) includes 16 tables, 101 figures and 107 references cited. In the introduction, the objectives of investigations are formulated and the state-of-art of the problems under investigation is described.

In the first chapter the technological process in fabrication of power thyristors and diodes is considered. Static and dynamic electrical parameters are characterized in more details. The principles of device operating conditions and related technology problems are discussed.

In the second chapter the technological steps in the formation of isolation grooves are discussed. The filling of isolation grooves with glass SiO_2-PbO-Al_2O_3-B_2O_3 at high temperatures is described. The passivation technique using diamond-like carbon (*a*: C-H) is presented. Development of passivation by porous silicon in isolation grooves is characterized in more details. Surface recombination and homogeneity measurement techniques are presented.

In the third chapter main results and discussions are presented.

3.1 Improvement of chemical etching in the formation of isolation grooves

In this chapter the main parameters of wet chemical etching of isolation grooves are discussed.

As substrates, n-type Si wafers of resistivity 60 to 120 Ω·cm, diameter ∅ 125 mm, thickness 0.37 mm, and (111) crystallographic orientation were used. The p-n junctions in the diode and thyristor structures have been formed by diffusion of boron and phosphorus for producing the p- and n-type regions, respectively. The resulting carrier concentrations in p- and n-type regions were 1×10^{14} to 2×10^{18} and 6×10^{13} cm^{-3}, respectively. The arrays in wafers were separated by isolation grooves formed by wet chemical etching technique. Commonly, the grooves of 100 μm in depth and 800 μm in width were etched using HF : HNO_3 : CH_3COOH [(3-1.7) : (2-4) : (0.7-2) (v/v)] mixtures. In a further technological process, the grooves were filled with SiO_2-PbO-Al_2O_3-B_2O_3 compound, which was melted into the glass by heating at 750 - 760°C.

The composition of chemical mixture influences on etching parameters of isolation grooves. Two etching apparatus are described, and their parameters are compared. By using the first apparatus, the depth distribution of isolation grooves 8.23 μm per wafer was obtained. The etching in the second apparatus gives the depth distribution of isolation grooves 0.95 μm per wafer. By this reason, the second etching apparatus has been selected for futher experiments. The second etching apparatus is shown in Fig. 1.

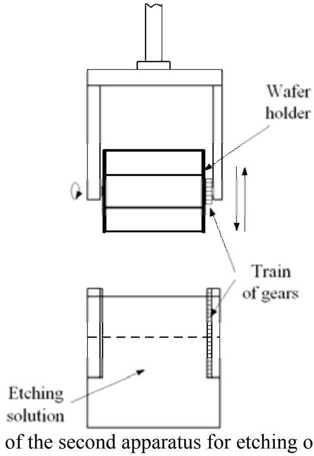


Fig. 1. The scheme of the second apparatus for etching of isolation grooves.

In processing of high-power Si devices, the quality of the etching process is characterized by the range *R* of the depth values and the profile of isolation grooves in wafer. The *R*-values influence on mechanical characteristics of wafer, such as hardness, which are important in a further technological procedure.

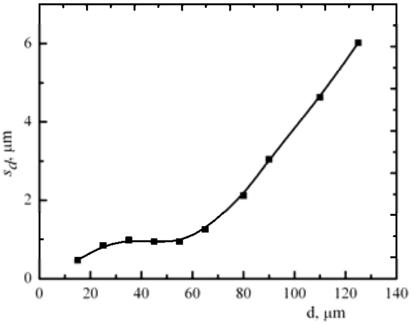


Fig. 2. Dependence of the standard deviation in depth values on the depth *d* of isolation grooves formed by wet-etching technique at etching cell rotating with a speed of 38 rpm. The curve is a guide to eye.

Experimental data have shown that *R*-values as well as standard deviation s_d (Fig. 2) increased with increasing *d*-values. The s_d-values presented in Fig. 2 were determined for isolation grooves formed on Si wafers etched at a standard speed of 38 rpm. As is seen from Fig. 2, the depth-dependence of s_d is a non-monotonous function with a particular point at *d*~70 µm corresponding to the location of the p-n junction. The s_d-values are almost independent on depth in the p-type region whereas a steep increase is noticed in the n-type region. This observation is in agreement with the etching rate for p- and n-type Si. A low etching rate in p-type Si has led to a low values of *R* and s_d whereas in the n-type region at larger *d*-values, a higher etching rate caused an increase of s_d values.

It is reasonable to assume that (i) nitric acid, as oxidizing agent, generates two holes and oxidizes the surface Si atoms to Si^{2+} and (ii) fluoric atoms replace hydrogen atoms on H-passivated Si surface.

As noted above (Fig. 2), experimental data have shown that standard deviation of the depth of isolation grooves is almost constant in the p-type Si region indicating a low etching rate. However, the etching rate is strongly dependent on carrier concentration, which varies by four orders of magnitude in the p-type region of high-power Si devices under consideration. It is reasonable to assume that hydrogen atoms, which have been originated as the reaction products, penetrate into Si during etching process and passivate dopant boron atoms leading to a formation of a high-resistivity layer. As a result, the etching rate is low leading to low s_d-values of the depth of isolation grooves. An increase of s_d-values in the n-type region can be explained by increased etching rate due to the absence of hydrogen passivation effect.

In order to decrease the range of *d*-values over the wafer, the dependence of standard deviation s_R on the rotation speed of etching cell v_{ec} was examined. For this purpose, the mechanism of train gears in the etching cell was improved to increase the rotation speed of the etching cell. However, the rotation speed was limited to v_{ec}~60 rpm because of the construction of apparatus.

Experimental data have shown (Fig. 3) that the isolation grooves were quite uniform in depth at higher v_{ec} - values. Therefore, it was proposed to increase the rotation speed of the etching cell up to 52 rpm. The increase of v_{ec} from 30 to 52 rpm resulted in the decrease of standard deviation s_R from 1.74 to 0.85 µm.

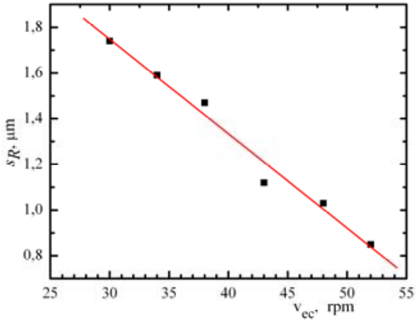


Fig. 3. Dependence of the standard deviation of the depth range s_R on the rotation rate of etching cell v_{ec} at a constant depth d =100 µm of isolation grooves.

An increase of rotation speed v_{ec} of etching cell resulted in the increase of the etching rate (Fig. 4). For example, the etching rate increased from 13.6 to 18.6 µm/min at the increase of rotation speed from 30 to 52 rpm. This dependence is caused by the enhanced homogeneity of the etchant and a more efficient removal of reaction agents at the local wet etching process. As a result, the etching rate was increased and it was more homogeneous over the wafer.

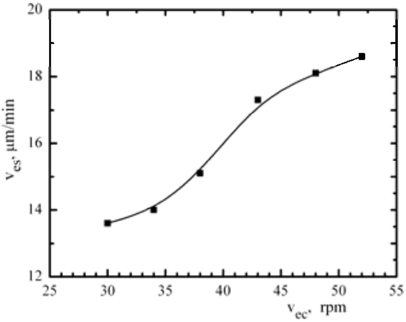


Fig. 4. Dependence of etching rate v_{er} on the rotation speed v_{ec} of etching cell at a constant depth d =100 µm of isolation grooves. The curve is a guide to eye.

The increase of v_{ec} has also resulted in the improvement of the profile of isolation grooves. The bottom of the isolation groove is smoother at higher rotation speed of the etching cell. The improvement of morphology is mainly due to an easier removal of the reaction products.

In the formation of isolation grooves, the dependence of etching characteristics on the temperature variation of etching mixture was investigated. In this series of experimental run, silicon wafers were etched at different temperatures of etching mixture at constant etching duration t=110 s. Initial protective SiO_2 film thickness was d_0 = 1.42 µm.

Table 1. The isolation groove depth and SiO_2 film thickness after etching procedure

Wafer No.	Temperature of etching mixture, °C	Depth, µm		SiO_2 thickness, µm	
		$\overline{X}$	R	$\overline{X}$	R
10	9.1	21.60	1.61	1.22	0.01
11	14.3	30.01	1.57	1.17	0.01
12	19.5	33.69	1.45	1.12	0.01
13	25.8	36.59	1.82	1.06	0.02
14	30.9	37.36	2.42	1.01	0.01

The results on the investigations on the depth of isolation grooves and SiO_2 film thickness after etching procedure are summarized in Table 1. An increase of the mixture temperature leads to an increase on the range of isolation groove depth, but it is not so significant for SiO_2 film thickness.

Isolation groove depth depending on etching mixture temperature is shown in Fig. 5 a. Increasing etching mixture temperature, grows etching rate of isolation groove and protective SiO_2 film at the same etching duration.

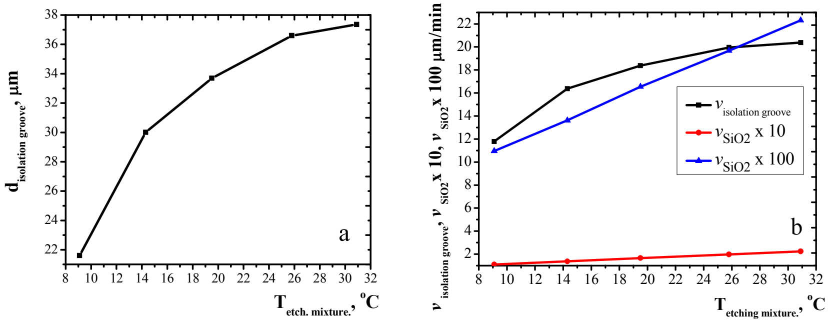


Fig. 5. Dependence of the isolation groove depth (a) and etching rate of isolation grooves and SiO_2 (b) on the temperature of etching mixture.

The ratio between the etching rates of isolation grooves and SiO_2 film indicates the selectivity of etching mixture. This value for Si/SiO_2 is important for formation process of isolation grooves and shows the thickness of SiO_2 film, which is necessary for the etching of a given depth of isolation grooves. Figure 5 b shows how Si and SiO_2 etching rate depends on the temperature of etching mixture. In Fig. 5b the SiO_2 etching rate is multiplied by 10 and 100 in order to illustrate the trends in the etching process. For both isolation grooves and SiO_2, the etching rate increases with an increase of the temperature of etching mixture. The etching rate of isolation grooves is 16.4 and 18.4 µm/min at 14.3 and 19.5°C, respectively.

3. 2 Improvement of glass SiO_2-PbO-Al_2O_3-B_2O_3 passivation

For improvement of the glass SiO_2-PbO-Al_2O_3-B_2O_3 passivation process, the monitoring system (Fig. 6) for the control of the glass passivation parameters was developed. This system allows one to observe the variation of the temperature and gas flows during the glass melting process.

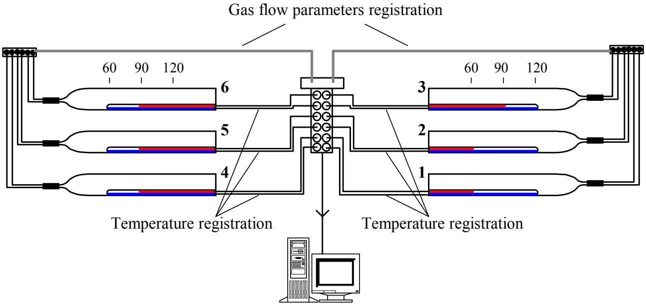


Fig. 6. The scheme of monitoring system for observation of the glass passivation process.

The observation system registers parameters from six glass passivation tubes and all the data are stored in the computer memory. In Fig. 7 the glass melting temperature profile is shown. The black and green curves show correspondingly the time variation of temperature at 120-cm and 90-cm points of the tube, when the glass in 50 wafers is melted.

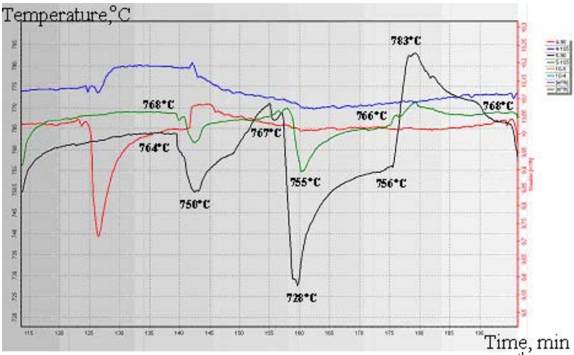


Fig. 7. The temperature profiles (black curve - temperasture at the 90th point of tube, green curve - temperasture at the 105th point of tube) during the glass melting procedure.

In all these 50 wafers the depth and the range of isolation grooves were measured over the wafers (5 points per wafer) by means of Stylus Profiler Dektak 6M. These wafers were etched in two processes and situated in glass melting process by the range from № 1 to № 50. In Fig. 8 is shown the range of isolation groove depth (numbers at blue points) and how the wafers were situated in glass melting process.

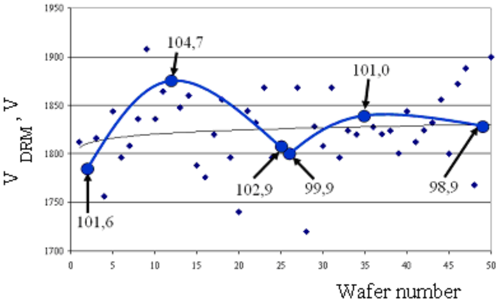


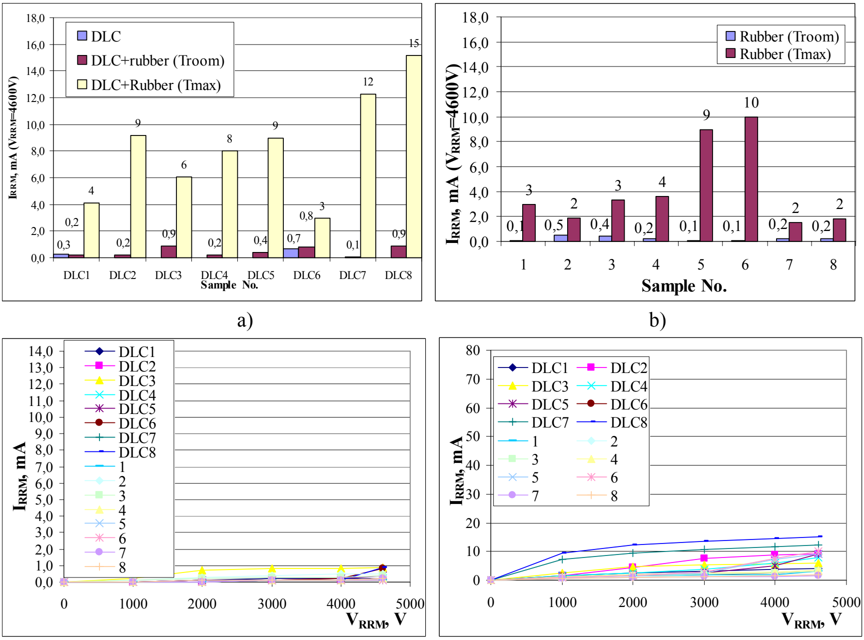
Fig. 8. V_{DRM} dependence on isolation groove depth and how were situated wafers during SiO_2-PbO-Al_2O_3-B_2O_3 glass melting process.

V_{DRM} (repetitive peak direct voltage) values repeats the range of isolation groove variation, independently how the wafers were situated during glass melting process. The isolation groove depth determines the value of breakdown voltage and glass melting process – breakdown voltage shape.

3. 3 Passivation by diamond-like carbon (*a*:C-H) films

The aim of this chapter was to present the results of the investigations with diamond-like carbon (DLC) films, those were used for the passivation of the edge in power thyristors and diodes. The main indicator of passivation efficiency is a leakage current at room and high temperatures. XPS and Raman spectroscopy have been also carried out for estimation of sp^2/sp^3 hybridization in DLC films.

In this series of experimental runs, 8 samples were coated with DLC film and rubber whereas other 8 samples were coated with only rubber. Before rubber coating process, the samples were tested at $V_{RRM} = 4600$V. After coating procedure, the samples with rubber were measured at T_{room}=25°C and T_{max}=150°C. As seen from Fig. 9, the I_{RRM} values of the samples with DLC are equal to standard rubber passivation group values.



a)

b)

c)

d)

Fig. 9. Control testing (at V_{RRM}=4.6 kV) results for samples coated with DLC, DLC plus rubber (a) and rubber (b) and I_{RRM} dependence on V_{RRM} for all samples at T_{room} = 25°C (c) and T_{max} = 150°C (d).

I_{RRM} dependences on V_{RRM} have shown (Fig. 9) that current values for samples with DLC are equal to those covered with standard rubber layer. Hence, the DLC-coating is suitable method for the reduction of leakage current, though it is necessary to find out the optimal production technology.

The structure of diamond like carbon is irregular with C atoms bound together by the sp^2 and sp^3 hybridizations. The presence of the sp^3 bonds is responsible for mechanical strength. Meanwhile sp^2 relation controls electric and optic characteristics. The ratio of carbon atoms with sp^2/sp^3 hybridization is a fundamental parameter that determines the physical properties of DLC films. The sp^2/sp^3 ratio can be estimated by X-ray photoelectron spectroscopy (XPS) and Raman scattering methods.

The next series of two samples were investigated. The sample 00L represented Si-silicon oxide surface without DLC and in the sample 3L (DLC6) silicon surface was covered with DLC film. The surface composition of these samples: 00L C – 91.6%, O – 8.1%, Si – 0.3% and 3L C – 86.2%, O – 13.8%. The oxygen was found on the surface and it is not adsorbed molecular oxygen, but formative chemical relations with carbon. This result has been confirmed by carbon C 1s X-ray photoelectron spectrum, in which carbon having bonds with oxygen atoms was clearly separated (Fig. 10).

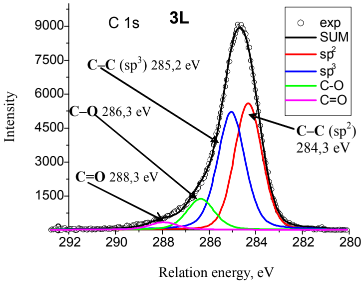


Fig. 10. C 1s X-ray photoelectron spectrum in the sample 3L. The points represent experimental results, continous lines show decomposition of the spectrum into components and their total contribution.

The hybridization of electron orbitals was evaluated by the areas of two peaks at 284.2 eV (sp^2 hybridization) and 285.2 eV (sp^3 hybridization). The results obtained on the investigated samples are presented in Table 2.

Table 2. The results of studies of sp^3/sp^2 hybridization.

Sample	Curve area (peak 284.2 eV)	Curve area (peak 285.2 eV)	sp^2 hybridization, %	sp^3 hybridization, %	Ratio sp^3/sp^2
00L	13113.5	6917.4	**65.5 %**	**34.5 %**	0.53
3L	8900.0	8700.0	**50.6 %**	**49.4 %**	0.98
graphite	13590.9	5270.6	**72.1 %**	**23.9 %**	0.33

Raman scattering measurements have been performed with excitation laser of wavelength 325 nm. Raman spectrum of the investigated sample 3L is shown in Fig. 11. In most of Raman scattering spectra, which have been measured in the range from 700 to 2100 cm^{-1}, two bands at ~1600 cm^{-1} (G band) and 1350 cm^{-1} (D band) dominate. The first band is related to graphite structure. The sample 3L was annealed at 420°C in H$_2$-atmosphere and Raman scattering spectrum was repeatedly measured. After annealing, in the sample 3L a weak band at 1940 cm^{-1} was found and increased intensity at 1420 cm^{-1} was observed (see Fig. 11). These observations indicated in the picture with continous and dashed lines and it may be caused of reduced thickness of tested film.

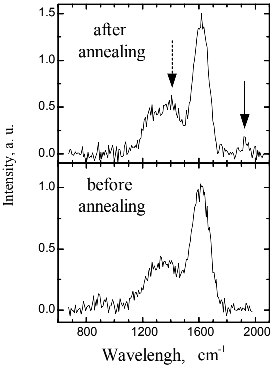


Fig. 11. The Raman scattering spectrum of sample 3L. Experimental results before (bottom) and after (top) annealing are shown.

Table 3. The characterization of chemical bonds between carbon atoms in initial 3L sample and after annealing in H_2-atmosphere.

Sample	Curve area (peak 284.2 eV)	Curve area (peak 285.2 eV)	sp^2 hybridization , %	sp^3 hybridization, **%**	Ratio sp^3/sp^2
3L	8900.0	8700.0	**50.6 %**	**49.4 %**	0.98
3L annealed	3668.9	2318.0	**61.3 %**	**38.7 %**	0.63

Chemical bonds between carbon atoms in initial sample 3L and after annealing in H_2 atmsophere are characterized in Table 3. As it is seen, after annealing the sp^3-character of the bonds in the sample 3L was reduced. Annealing in the H_2 atmsophere does not reduce the quantity of carbon combined with oxygen. During annealing process, the erosion of the DLC film occurred as evidenced by reduction of the film thickness.

3. 4 Investigation of parameters of the surface recombination

In this chapter, the method for passivation control after each technological step was developed making use of the measurements of surface recombination characteristics by non-invasive technique employing microwave-probed photoconductivity transients (MW-PCT). The passivation of moat surface has been carried out in two procedures: (i) electrochemical etching leading to the formation of the hydrogen-rich porous silicon layer and (ii) glass in-melting technique. It has been shown that surface recombination velocity decreases from $3 \cdot 10^3$ cm/s to 10 cm/s. Thus, passivation quality approaches to that of suppressed surface recombination velocity obtained for silicon wafers exploiting the iodine ethanol solutions.

The microwave probed photoconductivity transients measured in the structures under investigation after various surface preparation procedures are illustrated in Fig. 12. Different carrier decay rates can be clearly deduced from the photoresponse transients normalized to the peak value attributed to various surface treatment procedures. The shortest effective lifetimes are obtained for non-passivated moat surface, while the longest ones are measured after in-melted glass. A pre-passivation by electrolysis procedure induces a slight increase of effective lifetime, while this effect disappears after long storage.

The effective lifetime variation under the processing mentioned above is shown in Fig. 13. The effective lifetime values measured within treated grooves (1) are compared with those obtained in wafer samples of nearly the same resistivity and technology for non-passivated surfaces and passivated by iodine solution (2) in Fig. 13.

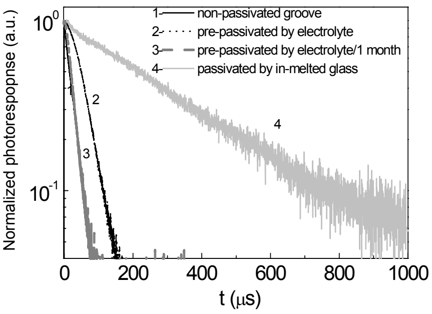


Fig. 12. Excess carrier density relaxation transients measured by MW-PCT technique within junction termination grooves for as–etched moat surface (1), for freshly pre-passivated by electrolyte (2) as well as after long storage of the pre-passivated groove surface (3), and for the passivated moat surface using in-melted glass (4).

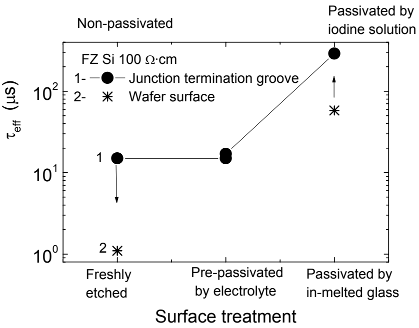


Fig. 13. Effective lifetime of the excess carrier decay under various surface treatments of the junction termination grooves (1) compared with those measured in non-passivated and passivated wafer samples of the initial Si material (2).

Effective thickness of d_{eff} = 60 μm for wafer samples has been defined rather precisely while this parameter is difficult to estimate for measurements in isolation grooves. Therefore, values of surface recombination velocity can be estimated more reliably by comparing effective lifetimes in wafers and grooves. From values of effective lifetimes, assuming parameters of carrier diffusion and effective thickness for wafer samples, the parameter *s* of velocity of the surface recombination is estimated to be of 100 cm/s for passivated and $5.5 \cdot 10^3$ cm/s for non-passivated surfaces, respectively. Thus, the values of s can be evaluated to be $s \approx 600$ cm/s for pre-passivated and $s \ll 100$ cm/s for groove surfaces passivated with in-melted glass. Long effective lifetimes of 300 μs measured in the grooves with in-melted glass indicate that carrier decay rate is governed by bulk recombination defects. It has been determined that in high resistivity Si wafers the long bulk lifetimes are inherent and passivation by iodine makes a very significant increase of effective lifetime to values of τ_b >350 μs. Surface recombination has been estimated to be s ≈ 10 cm/s in termination grooves with in - melted glass.

To verify the estimated *s* values in passivated grooves, the dual wavelength excitation regime has been employed in records of MW-PCT transients. No significant decrease (curve 4, Fig. 12) was detected within initial decay amplitude by changing excitation domain varying excitation wavelength from 1062 to 531 nm and by estimation of *s* values. This indicates that *s* values are really low for well passivated grooves. Surface recombination seems to be also suppressed by junction, when boundary surfaces of grooves are reliably isolated by in-melted glass.

3. 5 Porous silicon gettering and bulk passivation

In this chapter a new passivation scheme is proposed which is based on a formation of porous silicon layer for passivation of the surface of space charge region. These studies are focused on the development of a simple technique for a rapid formation of porous silicon layer as a passivation coating for typical crystalline silicon industrial power thyristors and diodes structures.

In the proposed technology, the *p-n* junction at the surface of grooves was passivated by porous silicon layers before glass-filling procedure. Porous silicon layers were formed electrochemically in fluoroplastic cell. The diode structures were etched in $HF:C_2H_5OH$ (1:1) electrolyte at electric current density (20-30) mA/cm^2 and etching time (20-180) s. The etching process was carried out in galvanostatic regime by means of *AUTOLAB, GPES-General Purpose Electrochemical System v 4.9*. As the anodized area contained the p-n junctions, i.e., the p- and n-type regions were simultaneously etched, the etched surface was illuminated by 100 W incandescent lamp (λ = 1.12 μm, 600 lx). After electrochemical process, the passivated diode structures were washed by distilled water, dried and annealed at 550°C in hydrogen atmosphere.

The main factor influencing the breakdown voltage is the presence of metal ions on the surface of p-n junction. The metal ions are adsorbed during the chemical processes like etching the grooves in acid solutions. An increase of HF concentration leads to the increase of adsorption of metal ions. When HF-concentration is 1.2 M, the concentration of adsorbed metal ions is 5×10^{15} cm^{-2}. An increase of HNO_3 concentration favors the oxidation of metal ions and solution of metal oxides. Adding acetic acid to etching solution allowed us to lower the concentration of adsorbed Fe, Ni, Co, Cd ions down to 5×10^{13} cm^{-2}. In addition, the porous silicon layer is known to possess the gettering feature. Therefore, it is reasonable to predict that passivation of p-n junction by porous silicon before glass-filling procedure will improve the characteristics of diode structures. It should be also emphasized that another important property of porous silicon is the gettering of the structural defects like dislocations leading to an increase of average yield of diode structures in industrial silicon wafers.

The biasing voltage was monitored during a single electrochemical layer fabrication to detect anomalies such as significant changes in voltage due to leakage. In Fig. 14 a typical voltage monitored during the etching is shown. The curve of particular shape was observed. The plot contains surprisingly many features for the sample etched with a constant current. There is a transient region in the beginning which may be ascribed to a build up of charge before etching begins, e.g. due to an activation energy.

The irregular saw-tooth pattern may be due to local oxide build-up and etching, as in the current-burst model or due to hydrogen bubbles interfering with electrolyte flow.

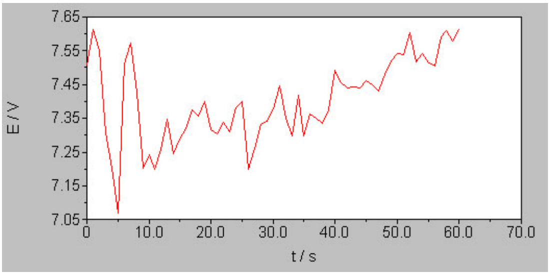


Fig. 14. Voltage variation during etching with constant cuurent (diagram of № 3 wafer).

Table 4. Average V_{RRM} values and ranges before and after electrochemical etching.

Before electrochemical etching				After electrochemical etching		
Wafer number	1.	2.	3.	1.	2.	3.
$\overline{X}_{V_{RRM}}, V$	1860.9	1807.2	1766.7	1909.6	1847.2	1900.0
$R_{V_{RRM}}, V$	2000	1600	1700	1100	1500	700

The breakdown voltage increased after etching by about 2.6%, 2.2% and 7.6% in wafers 1, 2, 3, respectively (see Table 4).

The results of passivation studies are summarized in Fig. 15. This figure shows the repetitive peak reverse voltage under various surface treatments of the junction termination grooves. The average U_{RRM} value of non-passivated isolation groove is 738 V, the range of values is 110 V. After electrochemical etching, the average V_{RRM} value is 759 V, the range of values 64 V (second treatment method). In the third tratment method the V_{RRM} value after SiO_2-PbO-Al_2O_3-B_2O_3 glass isolation groove passivation is shown. The latter value is 1815 V and the range of values is 134 V. Isolation groove passivated by electrolyte and SiO_2-PbO-Al_2O_3-B_2O_3 glass is shown in the fourth treatment level in Fig. 15. The efficiency of this method is about 90 V comparing with the third treatment method. The average V_{RRM} value for the samples passivated by this method reaches 1904 V with the range of values 156 V.

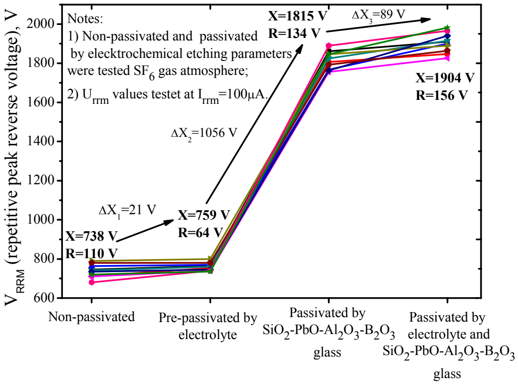
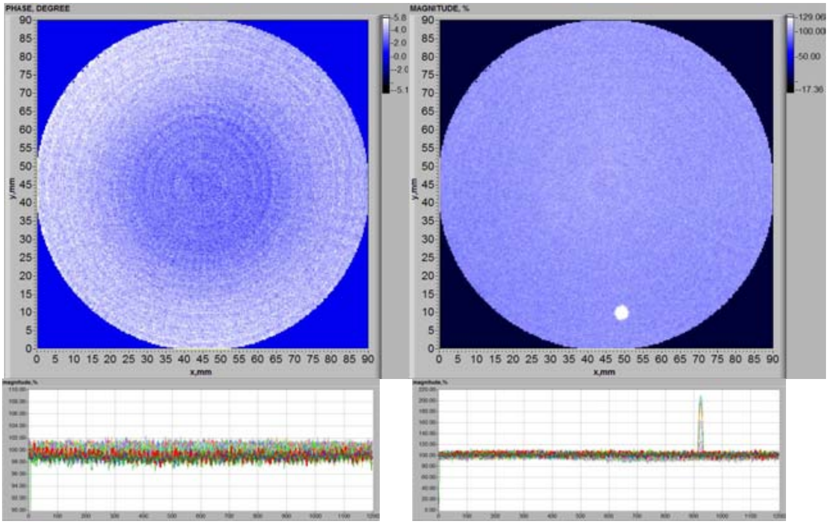


Fig. 15. Repetitive peak reverse voltage under various surface treatments of the junction termination grooves.

Testing of diode structures has shown that using passivation by porous silicon layer and glass passivation, an average breakdown values increase and an increase of yield of 8 % was estimated in the investigations of three ∅ 100 mm wafers with 69 cells of diodes in each.

3.6. Nondestructive homogeneity mapping of Si wafers by millimeter waves

The main idea of the experiment is the local excitation of millimeter waves and the measurement of the transmitted amplitude and phase in different places of the material under investigation. This investigation was perform on device which was produced in Semiconductor Physics Institute, Microwave Laboratory. It has been accomplished as a millimeter wave (f = 120 GHz) bridge consisting of the reference signal and the measurement channels. A silicon wafer under investigation is placed between dielectric waveguide probes, which provide local excitation and reception of the low power millimeter waves. The wafer can be moved by scanning mechanism with respect to the exciting and receiving probes in the x-y plane. Measured amplitude and phase of the transmitted wave depend on the value of the complex dielectric constant in the area, where the electromagnetic waves are excited. Therefore, by probing the wafer at different points with a millimeter wave beam, information about the homogeneity of the wafer is obtained. The measurement process is computer controlled and the measurement results are compiled in the computer. The example of the distribution of transmitted amplitude image for silicon is presented in the Fig 16.



a) b)

Fig. 16. The distribution of the amplitude of the microwave signal transmitted through the ∅125 mm Si wafer ($d = 0.4$ mm, scanning area 90 mm^2). The wafer before GaAl diffusion (a) and the wafer after GaAl diffusion (b).

The figure shows the same silicon wafer before and after GaAl diffusion. It is clearly seen that tested material is homogeneous. Before GaAl diffusion the range of amplitude and phase distribution is 4 % and after diffusion is about 8 %. This method is most useful for testing Si wafers after GaAl diffusion.

Conclusions

1. Power semiconductor device structural construction, the main characteristics, the relations between parameters and technological process were analysed.
2. The regularities of chemical etching of isolation grooves in the formation of power semiconductors have been investigated. For smooth etching is nessesary to keep ratio between HNO_3 and HF ~ 1,97. Basing on the results obtained, the optimal technology for the formation of isolation grooves was developed and new-construction device for selective chemical etching of semiconductor structure was developed.
3. The dependence of V_{DRM} and V_{RRM} parameters on SiO_2-PbO-Al_2O_3-B_2O_3 glass melting temperature variation was investigated. It was determined that the V_{DRM} values repeat the range of isolation groove variation, independently of how the wafers were situated during glass melting process. The isolation groove depth causes the value of breakdown voltage and glass melting process – breakdown voltage shape.
4. I_{RRM} dependence on V_{RRM} indicated that the current values in samples with DLC are equal to those for samples covered with standard rubber layer. This DLC-coating method is suitable for reducing the leakage current values, though it is necessary to optimize the technology conditions during production process.
5. The surface recombination velocity s decreases from $\sim 3 \cdot 10^3$ cm/s to ≤ 10 cm/s under different surface treatments of junction termination grooves. Effective carrier lifetime in well-passivated grooves approaches to bulk recombination lifetime in the initial Si material.
6. Gettering and hydrogenation ability of porous silicon films were used to improve the breakdown voltage of high voltage silicon diodes. The investigations of three ∅ 100 mm wafers with 69 cells of diodes in each have shown an increase of yield of 8% using the passivation by porous silicon layer.
7. Before diffusion the range of the amplitude and phase distribution is 4 % and after diffusion is about 8 %. Nondestructive homogeneity mapping of Si wafers by millimeter waves method is useful for testing only after diffusion, because testing after other operations is not informative, the signal disappears in the noise of signal.

List of publications

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2. E. Gaubas, T. Čeponis, D. Šalucha, I. Šimkienė, A. Uleckas. Characteristics of Surface Recombination in Silicon Diode Isolation Grooves. Lithuanian Journal of Physics, Vol. 47, No. 4, p. 461 - 464 (2007).
3. D. Šalucha, A. Marcinkevičius. Investigation of Porous Silicon Layers as Passivation Coatings for High Voltage Silicon Devices. Electronics and Electrical Engineering Nr. 7 (79), p. 41 – 44 (2007).
4. D. Šalucha, I. Šimkienė, J. Sabaitytė. Formation of Nanostructured Layers for Passivation of High Power Silicon Devices, Acta Physica Polonica A Vol. 113 – No. 3, p. 1079 – 1083 (2008).
5. D. Šalucha, I. Šimkienė. Isolation Groove Wet Chemical Etching Characteristics of Silicon High-Power Devices, „Science-The Future of Lithuania“, Physics and Physical Computer Science No. 1 (3), (2009).
6. D. Šalucha, I. Šimkienė, Problems of wet chemical etching of isolation grooves in high-power silicon devices, Lithuanian Journal of Physics, (2009) accepted.

Reziumė

Šiame darbe išanalizuota galingų puslaidininkinių struktūrų konstrukcija, pagrindinės charakteristikos, parametrų tarpusavio ryšis, taip pat technologinis procesas ir jo ypatumai. Išanalizuotos technologinio gamybos maršruto silpniausios pozicijos. Nustatyta izoliacinių griovelių ėsdinimo charakteristikų priklausomybė nuo ėsdiklio sudėties, nuo ėsdinimo įrenginio struktūros, nuo ėsdiklio temperatūros kitimo. Tolygiam ėsdinimui turi būti išlaikytas oksidanto (HNO_3) ir oksido tirpiklio (HF) santykis ~ 1,97. Sukurta ėsdinimo technologija yra panaudota naujoje ėsdinimo įrenginio konstrukcijoje, kurioje reguliuojamas ėsdinamų plokštelių sukimosi greitis bei kontroliuojamas ėsdiklio pašalinimas nuo plokštelių paviršiaus. Sukurta stiklo pasyvacijos difuzinės krosnies monitoringo sistema, kuri skirta aukštų temperatūrų ir dujų srautams matuoti. Nustatyta V_{DRM}/V_{RRM} parametrų verčių priklausomybė nuo SiO_2-PbO-Al_2O_3-B_2O_3 stiklo lydymo proceso: pramušimo įtampų vertės atkartoja griovio gylio pasiskirstymus nepriklausomai nuo plokštelės padėties stiklo lydymo temperatūrinėje zonoje. Griovelio gylis apsprendžia pramušimo įtampos vertę, o stiklo lydymo procesas – pramušimo įtampos charakteristikos pavidalą. DTAD plėvelės atkaitinimas vandenilio atmosferoje anglies, surištos su deguonimi, kiekio nesumažina, iškaitinimo metu vyksta plėvelės erozija, pasireiškianti plėvelės storio mažėjimu - šį faktą patvirtino abu tyrimo metodai. DTAD plėvelių izoliacinės savybės buvo vertintos pagal paviršinio elektrinio krūvio susikaupimą. Apsaugines DTAD plėvelės savybes taip pat lemia anglies cheminio ryšio charakteris. Nustatyta, kad DTAD plėvelės struktūra turi pasižymėti dideliu kiekiu anglies su ryškiai išreikštu sp^3 ryšio charakteriu ir mažu kiekiu anglies su grafitui būdingu sp^2 ryšio charakteriu. Rekombinacijų charakteristikų kitimo pagalba, matuojant bekontakte MW-PCT technika, įvertinta griovelių pasyvacijos kokybė. Gauta, kad pasyvuojant ir izoliuojant griovelio paviršių, krūvininkų efektinė gyvavimo trukmė kinta nuo 10 μs iki 300 μs. Tai atitinka paviršinės rekombinacijos spartos sumažėjimą nuo 3×10^3 cm/s iki 10 cm/s, priklausomai nuo griovelio krašto paviršiaus paruošimo metodo. Galingų puslaidininkinių prietaisų technologiniame gamybos maršrute po izoliacinio griovelio ėsdinimo operacijos prieš stiklo pasyvaciją sudarinėjamas porėtojo silicio sluoksnis. Nustatyta, kad ilgėjant ėsdinimo trukmei, didėja porėtojo silicio storis. Kadangi stipriai legiruotose sluoksniuose papildomai atsiranda sanglaudos defektų, lėtai aušinant defektai pereina į plevelę ir po to pašalinami kartu su ja. Tuo pačiu pašalinami ir gerai tirpstantys plėvelėje greitai difunduojančių metalų jonai (Au, Cu, Fe ir Ni). Šio metodo efektyvumas siekia 2 ÷ 8%, priklausomai nuo elektrocheminio ėsdinimo trukmės. Galingų puslaidininkinių prietaisų technologiniame gamybos maršrute siūloma įvesti homogeniškumo tyrimą milimetrinių bangų pagalba. Iš atliktų homogeniškumo tyrimų milimetrinių bangų pagalba, nustatyta, kad šie matavimai tikslingi skenuoti pradines plokšteles ir plokšteles po GaAl difuzijos, nes tik po šio proceso stebimi žemi triukšmų lygiai. Šie triukšmų lygiai išauga po kiekvienos operacijos ir homogeniškumas stebimas tik sudarytose skirtingo laidumo srityse. Įdiegus tokią matavimo metodiką į technologinį procesą, palengvėja broko paieška ir jo nustatymo vietos technologiniame gamybos maršrute.

Curriculum Vitae

Name, Surname	Dainius Šalucha
Birth date and place	15 December, 1979, Baisogala, Radviliškis district, Lithuania

Education:

1998 - Graduation certificate of secondary school

1998 – 2002 - Bachelor's degree, Faculty of Electronics, speciality of Electronic Equipment and Computer Hardware, Vilnius Gediminas Technical University.
Bachelor thesis: "Studies of powerful round thyristor parameters".

2002 – 2004 - Master degree, Faculty of Electronics, speciality of Electronic Equipment and Computer Hardware, Vilnius Gediminas Technical University.
Master thesis: "Studies of electrical characteristics in semiconductors alloy".

2004 – 2008 – PhD student, Semiconductor Physics Institute.

Work experience:

Stock Company "Vilniaus Ventos Puslaidininkiai" (Vilnius Venta Semiconductors), Ateities 10, LT-2057, Vilnius, Lithuania, www.vvp-uab.lt.

2002 – 2005 Process Engineering in:

- Alloy diodes line;
- Wafer sawing line;
- Diodes testing.

2005 - 2009 A Head of Glass Passivation Line.