VILNIUS UNIVERSITY
FACULTY OF PHYSICS
INSTITUTE OF APPLIED ELECTRODYNAMICS AND TELECOMMUNICATIONS

Adomas Jaras

MULTIBAND TUNABLE BANDPASS FILTER FOR FULLY DIGITAL SATELLITE TRANSCEIVERS

MASTER THESIS

Electronics and Telecommunication Technologies study programme

Student	Adomas Jaras
Allowed to defend	2024–05–23
Work supervisor	Mantas Sakalas
VU consultant	doc. Šarūnas Svirskas
Head of the institute	prof. Robertas Grigalaitis

Vilnius 2024

Santrauka

Adomas Jaras

DAUGIAJUOSTIS DERINAMASIS JUOSTINIS FILTRAS, SKIRTAS SKAITMENINIAMS PALYDOVINIAMS SIŲSTUVAMS – IMTUVAMS

Augantis didelio greičio ir mažos delsos internetinio ryšio poreikis visame pasaulyje skatina patikimų ir perkonfigūruojamas palydovinių ryšių sistemų vystymą. Tarp šių sistemų Žemosios Žemės Orbitos (ang. Low Earth orbit, LEO) palydovai atlieka svarbų vaidmenį plečiant ryšio galimybes. Šie ŽŽO palydovai remiasi programine įranga apibrėžto radijo (ang. Software Defined radio, SDR) technologija, kuri iš esmės priklauso nuo perkonfigūruojamų įrenginių. RF filtrai yra kritiški SDR imtuvo komponentai. Tradicinės technologijos nesugeba patenkinti tiek derinimo, tiek integravimo reikalavimų. Ši situacija motyvuoja šio darbo poreikį: sukurti aukštos kokybės, kompaktišką ir integruotą derinamą juostinio pralaidųjį filtrą, kuris apimtų tiek K, tiek Q juostas vienu metu.

Darbo tikslas – išnagrinėti daugiajuosčio derinamojo juostinio filtro įgyvendinimo galimybes kylančioms SDR ryšių sistemoms, užtikrinant ŽŽO veiklos standartų laikymąsi. Techniniai tikslai apima mažus įterpimo nuostolius, didelę integraciją ir K bei Q dažnių juostų aprėptį. Be to, projektuojamas įtaisas siekia palaikyti siaurą 3 dB juostos plotį ir užtikrinti didelį signalo slopinimą už juostos ribų.

Metodika, naudojama siekiant nustatyto tikslo, apėmė filtro schemos projektavimą ir jos simuliaciją. Įterpimo nuostoliai kiekvienoje filtro grupėje nustatė stiprintuvams keliamą stiprinimo vertės tikslą, ir, remiantis tuo, buvo suprojektuotas vieno ir dviejų pakopų stiprintuvas K ir Q juostoms atitinkamai. Pasiekus norimus rezultatus schemų projektavimo etape, validacija perėjo prie išdėstymo simuliacijos. Rezultatai atskleidė didžiausią nukrypimą veikimo srityje už juostos ribų, o veikimas juostos viduje liko pastovus. Galiausiai rezultatai buvo palyginti su mokslinėje literatūroje esančiais duomenimis, ir buvo padaryta išvada, kad filtras yra konkurencingas savo techniniais parametrais, taip pat užima mažesnį lusto plotą ir apima dvi juostas vienu metu. Tai daro šį darbą reikšmingu elektronikos inžinerijos srityje, nes toks sprendimas dar nebuvo pasiūlytas.

Table of contents

List of Abbreviations

LEO – Low Earth Orbit

SDR – Software-Defined Radio

RF – Radio Frequency

MTBF – Multiband Tunable Bandpass Filter

MMIC – Monolithic Microwave Integrated Circuit

CR – Coupled Resonator

PCB – Printed Circuit Board

K band – Frequency range from 18 to 27 GHz

Q band – Frequency range from 33 to 50 GHz

S-parameters – Scattering parameters

MOS – Metal-Oxide-Semiconductor

IBW – Instantaneous Bandwidth

dBc – Decibels relative to the center frequency

IIP3 – Input Third-Order Intercept Point

OP_{1dB} – Output 1 dB Compression Point

BiCMOS – Bipolar Complementary Metal-Oxide-Semiconductor

MEMS – Micro-Electro-Mechanical Systems

GaAs P-HEMT – Gallium Arsenide Pseudomorphic High Electron Mobility Transistor

GD – group delay

Introduction

The growing demand for high-speed, low-latency connectivity worldwide drives the need for reliable and adaptable satellite communication systems. Among these systems, Low Earth Orbit (LEO) satellites play a crucial role in expanding communication capabilities. These LEO satellites rely on emerging Software-Defined Radio (SDR) technology, which inherently depends on reconfigurable devices. RF filters serve as common and critical components in the SDR front-end. Traditional technologies for making tunable RF filters, such as ferrimagnetic resonators, micromechanical resonators, cavity resonators, varactor loaded planar resonators, offer excellent performance in few certain areas, fall short in meeting both tunability and integrability requirements [1]. Additionally, existing solutions that involve using a large number of non-tunable filters are impractical due to the significant chip dimensions they occupy [2] and the valuable PCB area they consume. This situation motivates the need for this thesis: to develop an on-chip, high-performance, compact tunable bandpass filter that can be highly integrated and would cover both K and Q bands simultaneously, a solution that has not yet been reported.

In this work, a design for a Multiband Tunable Bandpass Filter (MTBF) for emerging LEO SDR high data rate applications is investigated. The aim of this thesis is to explore the feasibility of designing a multiband tunable bandpass filter Monolithic Microwave Integrated Circuit (MMIC) for emerging SDR communication systems, ensuring compliance with LEO operational standards. The technical objectives include achieving low insertion loss, a high degree of integration, and coverage of the K and Q frequency bands used by emerging LEO communication systems. Additionally, the design aims to support a narrow tunable 3 dB bandwidth and provide high out-of-band signal rejection.

This thesis is organized as follows: following the motivation and objectives outlined in the introduction, Chapter 1 delves into the theory of high-frequency network analysis and introduces the principles of Coupled Resonator (CR) theory, which underpins the design of the Multiband Tunable Bandpass Filter (MTBF). At the end of Chapter 1, a review of the scientific literature on tunable passband filters in the K and Q bands will be presented. Chapter 2, the technical segment of the thesis, establishes the targeted project specifications. Chapter 3 presents the experimental part, detailing the design procedure for the filter banks and amplifiers. Chapter 4 showcases the schematic and post-layout simulation results, followed by a thorough discussion. Finally, the thesis concludes with a summary of the findings and their implications.

1. Theoretical part

1.1. Two and *n*-port circuit analysis

In the field of high-frequency electronics engineering, understanding the behavior of complex circuits is crucial for developing effective and reliable systems. The engineer's goal is to select the most appropriate type of parameters that describe the circuit to enable accurate analysis. Traditional linear circuit parameters used at low frequencies pose several challenges in the analysis and measurement of high-frequency circuits, mainly that the measurement of high-frequency voltages and currents in the laboratory proves very difficult, whereas that of average power is more straightforward [3]. For this reason, an alternative set of parameters, known as scattering or S-parameters, is introduced [4].

1.1.1. *S*-parameters

The advantage of S-parameters is that they are measured under controlled finite impedance conditions [5]. Transmission lines with a characteristic impedance of 50 Ω and broadband 50 Ω terminals can be reliably fabricated on alumina or semiconductor substrates, including silicon, at frequencies exceeding 300 GHz. Other broadband impedances with higher values that are precisely controlled can be produced as waveguide components. The mapping of S-parameters for any circuit is called a scattering matrix, and scattering parameters can be understood by examining incident, reflected, and transmitted signals as traveling waves. The matrix formulation of S-parameters is provided below [8]:

$$\begin{bmatrix} b_1 \\ b_2 \\ . \\ . \\ . \\ b_n \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & . & . & . & S_{1n} \\ S_{21} & S_{22} & . & . & . & S_{2n} \\ . & . & & & & . \\ . & . & & & & . \\ . & . & & & & . \\ S_{n1} & S_{n2} & . & . & . & S_{nn} \end{bmatrix} \times \begin{bmatrix} a_1 \\ a_2 \\ . \\ . \\ . \\ a_n \end{bmatrix} \quad (1)$$

where

$$S_{ij} = \frac{b_i}{a_j} [a_k = 0, \text{when } k \neq j]. \quad (2)$$

From equation (1), it can be seen that S_{ij}, indicating the transmission coefficient from port j to port i, is determined by directing an incident wave a_j into port j, and measuring the reflected wave b_i exiting from port i, while incident waves to all other ports except j are zero, and these ports are terminated with matched loads to prevent reflections. S_{ii} is the reflection coefficient at port i, when all other ports are terminated with matched loads. S-parameters are normalized with respect to the reference impedance Z_0. If we have a two-port network (Figure 1), the values of the S-parameters will be:

S_{11} – known as the input reflection coefficient or input return loss,

S_{12} – reverse gain or isolation between two ports,

S_{21} – forward transmission gain between two ports, and

S_{22} – output reflection coefficient or output return loss.

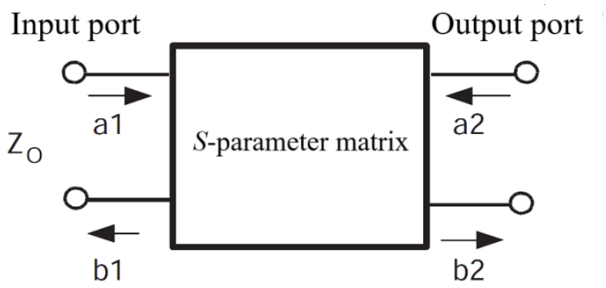


Figure 1. Definition of two-port *S*-parameters matrix [5]

1.2. Impedance matching

Traditional analog circuit design relies on strongly impedance mismatched circuit stages to maximize voltage or current gain. As an example, for maximum voltage transfer, the impedance of the load must be significantly larger than that of the driving stage. In contrast, for maximum current transfer, the load impedance must be much smaller than the impedance of the driving stage. Unlike at low frequencies where the signal wavelength exceeds one meter, at high frequency the electrical distance between circuit pads and external terminations becomes comparable to the signal wavelength. Impedance mismatches at either the near or the far end cause reflections that can significantly reduce the signal power arriving at the destination circuit.

To ensure maximum power transfer between the signal source and a device under test (DUT), the input impedance of the DUT Z_{in} must be conjugately matched to that of the signal source, Z_s. The same applies for the maximum power transfer from the DUT to its load. The output impedance of the DUT Z_{out} must be conjugately matched to the load impedance Z_L. Therefore, as illustrated in Figure 2, matching networks must be inserted between the amplifier and the signal source, and between the DUT and the load.

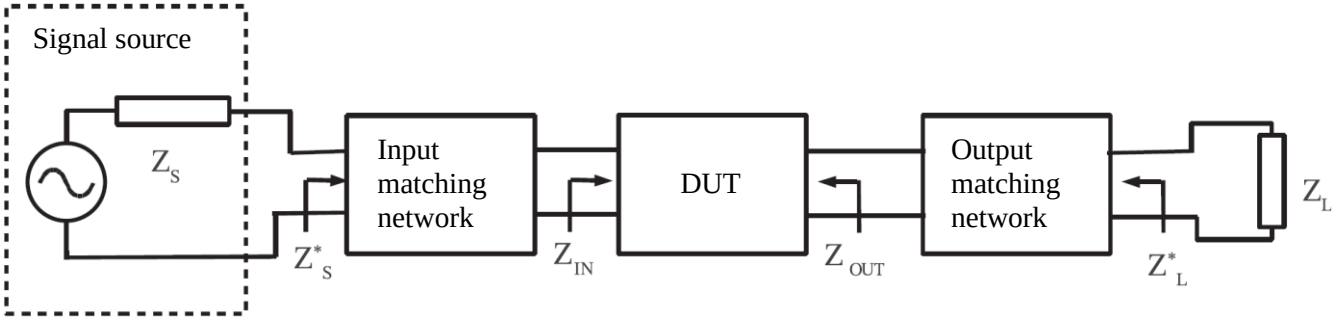


Figure 2. The principle of matching the input and output impedance of a DUT [5]

1.2.1. *L* type matching circuit

The simplest type of matching circuit is the *L*-section, which consists of two separate elements – a series reactance *jX* and a parallel reactance *jB*. There are two possible topologies, as shown in Figure 3 [8].

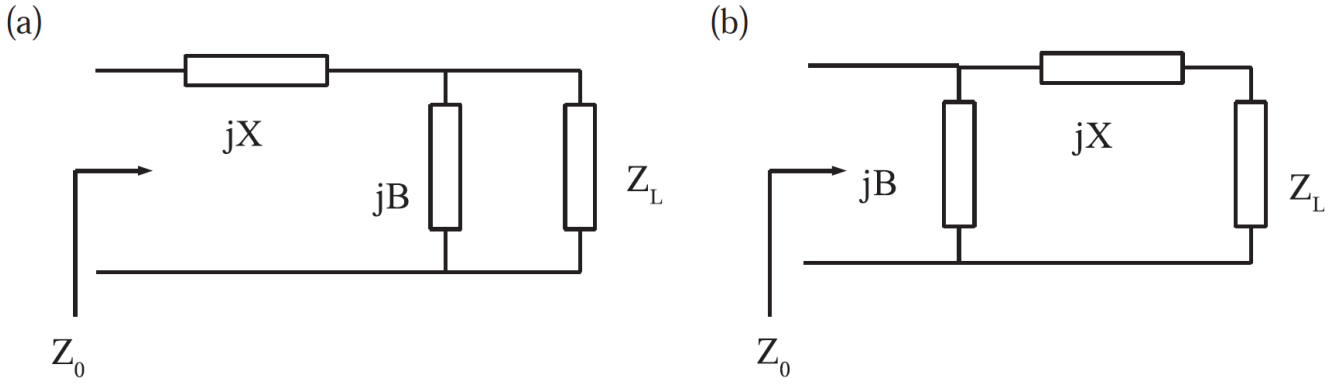


Figure 3. *L*-section matching circuit: a) when $Z_L < Z_S$ and b) when $Z_L > Z_S$ [5]

The choice of topology depends on the ratio of the source and load impedances. If $\frac{Z_L}{Z_S} < 1$, the configuration shown in Figure 3a will be used; if $\frac{Z_L}{Z_S} > 1$, the topology shown in Figure 3b will be used.

1.3. Coupled Resonator Filter theory

In the realm of integrated circuit design, achieving compact and tunable filters is a paramount challenge, especially as the demand for miniaturization and high performance continues to escalate. Among various filter design approaches, lumped *LC* components-based coupled resonator (CR) filters stand out as one of the viable options for creating highly compact and tunable on-chip filters. These filters leverage the inherent advantages of implementing alternating coupler and resonator topology, making them tunable by adjusting resonant frequency of the resonators or controlling the bandwidth by adjusting coupler. Consequently, lumped *LC* coupled resonator filters have become indispensable in the pursuit of advanced, miniaturized tunable filters in contemporary integrated circuit technology.

The objective of the following section is to present the principles of Coupled Resonator (CR) theory and identify the parameters that need adjustment to tune a filter while maintaining the desired frequency response. Initially, the chapter introduces impedance and admittance inverters, fundamental elements in CR theory, which facilitate the creation of a low-pass filter prototype that can be scaled in terms of impedance and frequency. It then explains how frequency transformation necessitates the use of resonators for bandpass filters, another key concept in CR theory. The relationship between coupling and filter bandwidth is analyzed. The chapter concludes by outlining the design process for tunable CR filters.

1.3.1. Insertion loss method

The modern approach to designing filters is known as the insertion loss method, which allows for the creation of filters with a fully specified frequency response. This process results in a low-pass prototype normalized for both frequency and impedance. By applying impedance and frequency transformations to this prototype, the desired frequency response and impedance matching can be achieved.

The low-pass prototypes of Butterworth and Chebyshev (all-pole) filters are designed as ladder networks consisting of series inductors and parallel capacitors, as illustrated in Figure 4. The Chebyshev filter is particularly popular because it offers the steepest cut-off rate among all-pole filters [6].

1.3.1.1. Impedance and Admittance Inverters

The theory behind Coupled Resonator filters is based on the inversion of an impedance or admittance. Networks performing such operation are called impedance (K) or admittance (J) inverters and are especially useful for bandpass or bandstop filters with narrow (< 10 %) bandwidths. The functionality of an inverter is described by equations (3) and (4) [7]:

$$Z_{in} = \frac{K^2}{Z_L} \tag{3}$$

where Z_{in} is input impedance, K is characteristic inverter impedance and Z_L is load impedance, and

$$Y_{in} = \frac{J^2}{Y_L} \tag{4}$$

where Y_{in} is input admittance, J is characteristic inverter admittance and Z_L is load admittance.

The principle of an inverter is illustrated in Figure 4.

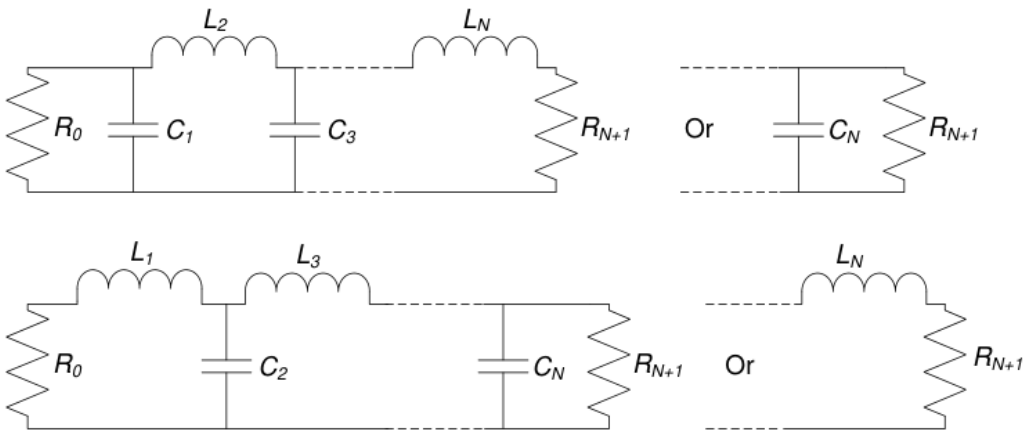


Figure 4. Two types of low pass ladder prototype networks

Admittance inverters are fundamentally the same as impedance inverters, but it is more practical to describe them using characteristic admittance rather than impedance. An inverter, a two-port network, inverts the terminating load (Z_L or Y_L) as shown in equations (3) and (4). The inverter is described by its characteristic impedance (K) or admittance (J). Besides, although not explicitly shown in equations (3) and (4) is that the inverter also changes the phase by $\pm\ 90^{\text{o}}$.

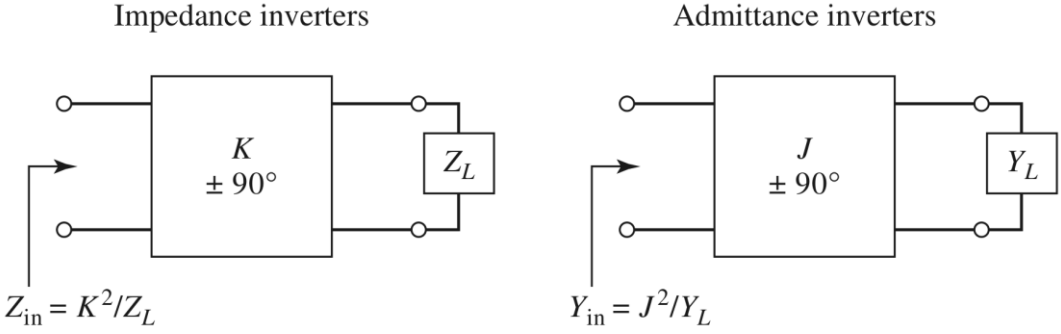


Figure 5. Operation of impedance and admittance inverters [7]

These equations demonstrate that the input impedance of an impedance inverter terminated with an inductor is capacitive. Similarly, the input admittance of an admittance inverter terminated with a capacitor is inductive. The inverter, being a lossless reciprocal two-port network, can be more broadly defined by transfer matrices [9].

$$[T_K] = \begin{bmatrix} 0 & jK \\ \frac{j}{K} & 0 \end{bmatrix} \tag{5}$$

$$[T_J] = \begin{bmatrix} 0 & \frac{j}{J} \\ jJ & 0 \end{bmatrix} \tag{6}$$

1.3.1.2. Inverters in a low pass prototype

When a series inductor is placed between two impedance inverters, the resulting transfer matrix is given by

$$[T_{network}] = \begin{bmatrix} 0 & jK \\ \frac{j}{K} & 0 \end{bmatrix} \cdot \begin{bmatrix} 1 & jX_L \\ 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} 0 & -jK \\ -\frac{j}{K} & 0 \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ \frac{jX_L}{K^2} & 1 \end{bmatrix} \quad (7)$$

This transfer matrix of the network is recognized as equivalent to a parallel capacitor with $Y_C = j\frac{Z_L}{K^2}$. Consequently, a low-pass prototype can be realized using only impedance inverters and series inductors, as these inverters can transform series inductors into parallel capacitors (see Figure 6). The dual network is constructed out of parallel capacitors and admittance inverters.

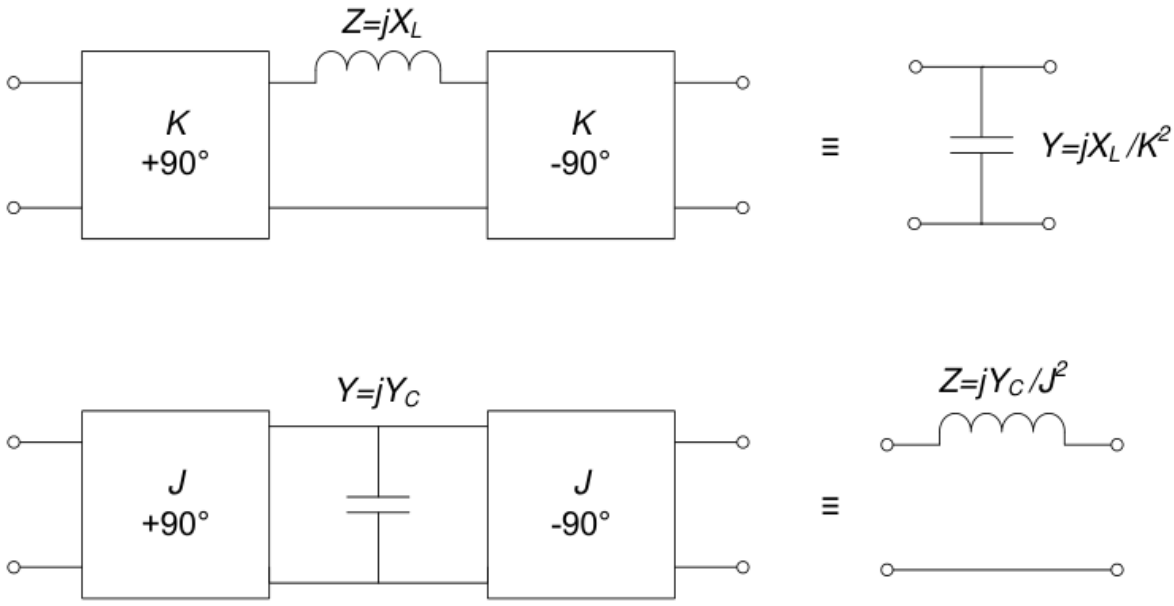


Figure 6. The depiction of an impedance inverter transforming a series inductor into a parallel capacitor and vice versa.

An alternative approach to realizing ladder networks can be achieved by leveraging the properties of impedance inverters, as discussed in reference [9]. This method involves utilizing coupled resonator low-pass prototypes, which are illustrated in Figure 7.

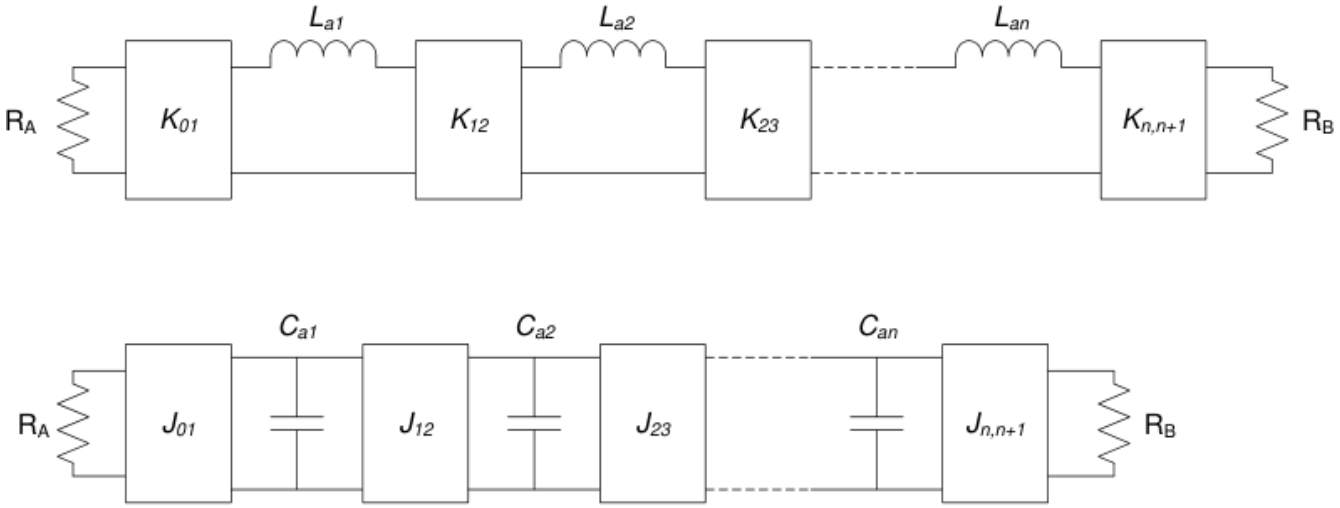


Figure 7. Two types of prototypes of a low pass coupled resonator networks

The inverters not only invert but also scale the impedance. This scaling simplifies matching at the terminating ports and provides an additional degree of freedom in the design. This flexibility allows for the use of identical reactive elements, leading to identical resonators in bandpass implementations. Identical resonators greatly simplify the design process, enabling the matching and optimization of multiple components simultaneously, which reduces computation time.

1.3.1.3. Bandpass transformation

A low-pass prototype network consisting of parallel capacitors and admittance inverters can be converted into a bandpass filter through a bandpass transformation. This transformation results in a network made up of parallel resonators and admittance inverters. A similar approach can be applied to create a bandpass filter using impedance inverters and series resonators. The specific bandpass transformation to convert low-pass filters into bandpass filters is as follows [10]:

$$\omega \leftarrow \frac{\omega_0}{\omega_1 - \omega_2}\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega_0}\right) = \frac{\omega_0}{\Delta\omega}\left(\frac{\omega^2 - {\omega_0}^2}{\omega_0 \omega}\right) \tag{8}$$

where ω_1 and ω_2 are the bandpass edges, and $\Delta\omega$ is the absolute bandwidth.

This transformation changes series inductors into series LC resonators and parallel capacitors into parallel LC resonators. These findings indicate that a bandpass CR filter consists of alternating resonator and inverter (coupler) sections, as illustrated in Figure 8.

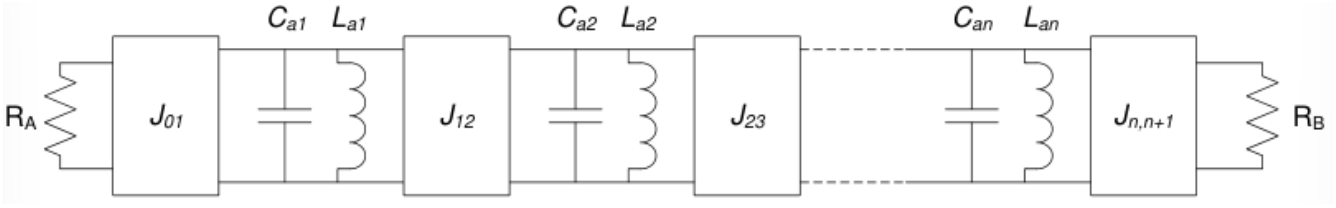


Figure 8. Bandpass prototype with coupled resonators using admittance inverters

1.3.2. Resonators

A resonator is a device designed to store energy in two distinct forms, and it functions by oscillating this energy between these forms. In an LC resonator, energy alternates between being stored as magnetic energy in the inductor and electric energy in the capacitor. Resonance occurs at a specific frequency where the average stored magnetic and electric energies are equal [10].

The resonant frequency can be adjusted by varying the average amounts of stored electric or magnetic energy, which, in an *LC* resonator, corresponds to changing either the inductance or the capacitance. There are various types of resonators, and it is useful to define the resonant frequency (ω_0) and the slope parameter to describe their resonance characteristics [8]. For resonators exhibiting series-type resonance, where the reactance is zero at ω_0, the reactance slope parameter is defined as follows:

$$\hat{x} = \frac{\omega_0}{2}\frac{dX}{d\omega}\bigg|_{\omega=\omega_0} \tag{9}$$

where X is the reactance of the resonator. In the case of parallel-type resonance, where the susceptance is zero at ω_0, the susceptance slope parameter is given by:

$$\hat{b} = \frac{\omega_0}{2}\frac{dB}{d\omega}\bigg|_{\omega=\omega_0} \tag{10}$$

where B is the susceptance of the resonator.

All non-ideal resonators exhibit some degree of loss, which is quantified by the unloaded *Q*-factor (Q_u). For series resonators, the *Q*-factor can be expressed as: [8]:

$$Q_u = \frac{\hat{x}}{R_s} \tag{11}$$

for series resonators, where R_s is the series resistance, and

$$Q_u = \frac{\hat{b}}{G_n} \tag{12}$$

for parallel resonators, where G_n is the parallel conductance [8].

The losses in resonators are particularly significant because they represent the primary source of loss in coupled resonator (CR) filters. At resonance, the circulating currents in the resonators are at their maximum due to the minimized impedance in the LC circuit. These losses are critical because the specifications (section 2.1) impose stringent requirements on attenuation in the passband. The effect of resonator Q factor on insertion loss and return loss in illustrated in Figure 9.

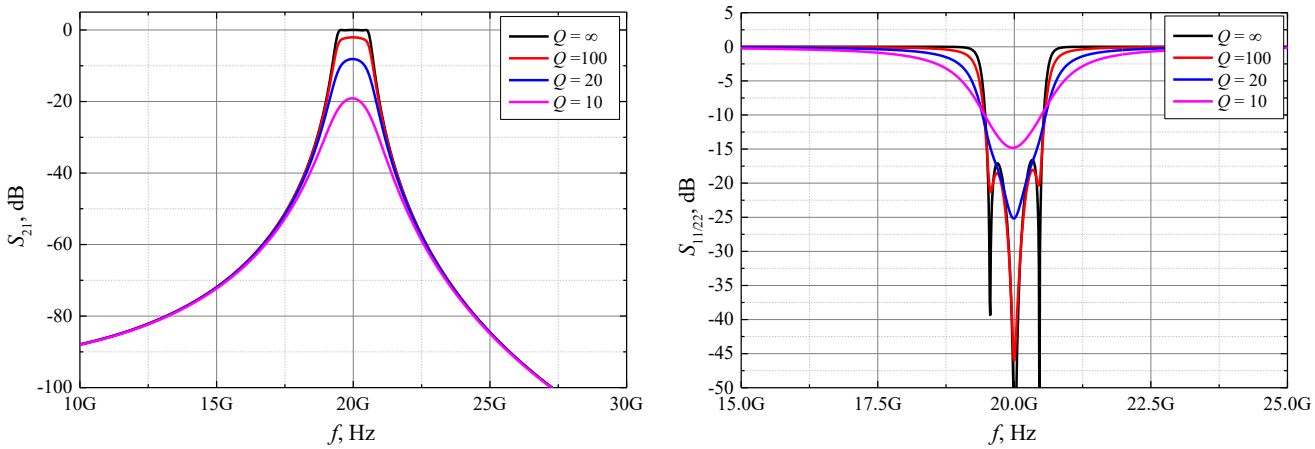


Figure 9. Dependance of filter transfer coefficient and return loss coefficient on resonator Q

1.3.3. Inter-resonator Coupling

In the design of lumped element filters, the concept of a coupling coefficient isn't strictly necessary, but it becomes a useful metric when considering bandwidth. Coupling is generally defined as the rate at which energy is exchanged between coupled resonators. This is evidenced by the fact that the coupling coefficient can be determined by analyzing the duration it takes for energy to enter and exit an electronic filter [11].

Coupling in electrical circuits arises due to mutual inductance or mutual capacitance, leading to inductive (magnetic) or capacitive (electric) coupling. Inductive coupling occurs when a change in current in one inductor induces a voltage in another conductor through mutual inductance (L_m).

$$v_2 = L_m \frac{di_1}{dt} \tag{13}$$

This is known as Faraday's law of magnetic induction. Capacitive coupling induces a current as a result of a voltage change.

$$i_2 = C_m \frac{dv_1}{dt} \tag{14}$$

Using equation (14) a two-port network can be constructed to show coupling with mutual capacitance.

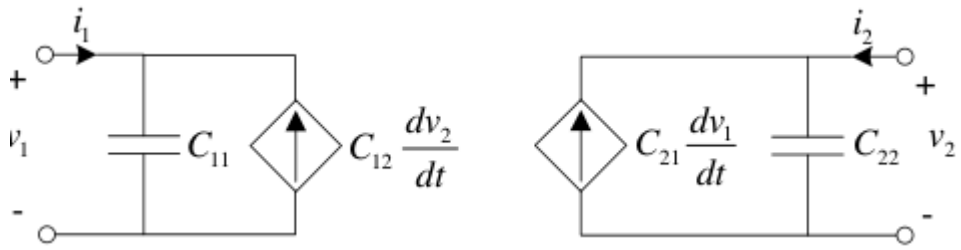


Figure 10. Coupling in two-port device with mutual capacitance

The mesh currents for the network given in Figure 10 are:

$$i_1 = C_{11}\frac{dv_1}{dt} - C_{12}\frac{dv_2}{dt} \tag{15}$$

$$i_2 = C_{22}\frac{dv_2}{dt} - C_{21}\frac{dv_1}{dt} \tag{16}$$

Transforming the network from the time domain to the frequency domain and writing it in matrix format, it gives:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} sC_{11} & -sC_{12} \\ -sC_{21} & sC_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{17}$$

A normalized variable, the coupling coefficient, can be defined to have the physical meaning of the amount of coupling [12],

$$k = \frac{L_m}{\sqrt{L_1 L_2}} \tag{18}$$

where L_1 and L_2 are the self inductances of the coupled conductors. Here, $k = 0$ indicates no coupling, while $k = 1$ represents maximum coupling. A similar definition applies to the capacitive coupling coefficient:

$$k = \frac{C_m}{\sqrt{C_1 C_2}} \tag{19}$$

Simplifications can be made where $C_{11} = C_{22} = C_0$ and $C_{12} = C_{21} = C_m$, leading to:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} sC_0 & -sC_m \\ -sC_m & sC_0 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{20}$$

The concept of capacitive coupling is illustrated by a circuit with two coupled capacitors, as shown in Figure 11. The portion of the circuit shown with dashed lines in Figure 11 represents an inverter, demonstrating that coupling can be achieved through an inverter circuit.

To understand the relationship between coupled resonators and the bandwidth of a filter, two *LC* resonators coupled with an inverter is analyzed. This configuration acts as a band-pass filter. For

simplicity, we assume the *LC* resonators are identical, without loss of generality. The mutual capacitance can then be expressed in terms of the coupling coefficient using equation (19):

$$C_m = kC_0 \tag{21}$$

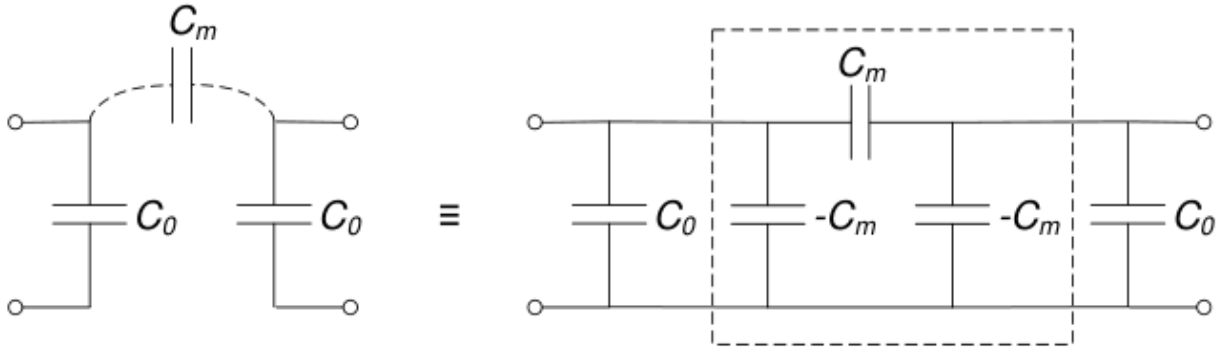


Figure 11. Capacitive coupling between two capacitors

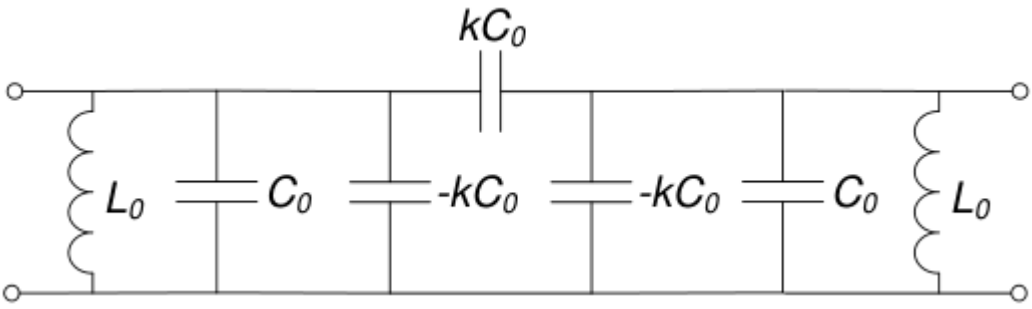


Figure 12. Coupled parallel *LC* resonators

The nodal equations for the network are:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} sC_0 + \dfrac{1}{sL_0} & -skC_0 \\ -skC_0 & sC_0 + \dfrac{1}{sL_0} \end{bmatrix} \cdot \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{22}$$

Using the admittance matrix, the input admittance of the network is:

$$Y_{in} = y_{11} - \frac{y_{12}y_{21}}{y_{22}} = \frac{(1-k^2)s^4{C_0}^2{L_0}^2 + 2s^2C_0L_0 + 1}{s^3C_0{L_0}^2 + sL_0} \tag{23}$$

Solving for the zeros of (23) gives the resonant frequencies of the system

$$s_{1,2} = \pm\frac{j}{\sqrt{C_0L_0(1-k)}} \tag{24}$$

$$s_{3,4} = \pm\frac{j}{\sqrt{C_0L_0(1+k)}} \tag{25}$$

These two zero pairs correspond to the odd and even resonant frequencies

$$\omega_{0o} = \frac{\omega_0}{\sqrt{1-k}} \tag{26}$$

$$\omega_{0e} = \frac{\omega_0}{\sqrt{1+k}} \tag{27}$$

where $\omega_0 = \frac{1}{\sqrt{C_0 L_0}}$. Solving for k using equations 26 and 27 gives

$$k = \frac{{\omega_{0o}}^2 - {\omega_{0e}}^2}{{\omega_{0o}}^2 + {\omega_{0e}}^2} \tag{28}$$

This equation provides insight into how changes in the coupling coefficient affect the system's frequency response. When the coupling (k) increases, the difference between ω_{0o} and ω_{0e} also increases. This means the resonant frequencies of the circuit (ω_{0o} and ω_{0e}) shift further away from the resonant frequency of the individual resonators (ω_0). Consequently, the bandwidth widens with increased coupling, as illustrated in Figure 13 [13].

The graph in Figure 13 shows the response of the circuit depicted in Figure 12 with varying coupling coefficients. It is clear from Figure 13 that stronger coupling results in a broader bandwidth. For this comparison, the load and source impedances were chosen as $R_L = R_S = \frac{1}{k}$. This choice maintains $Q_e k = 1$, ensuring a maximally flat (Butterworth) response.

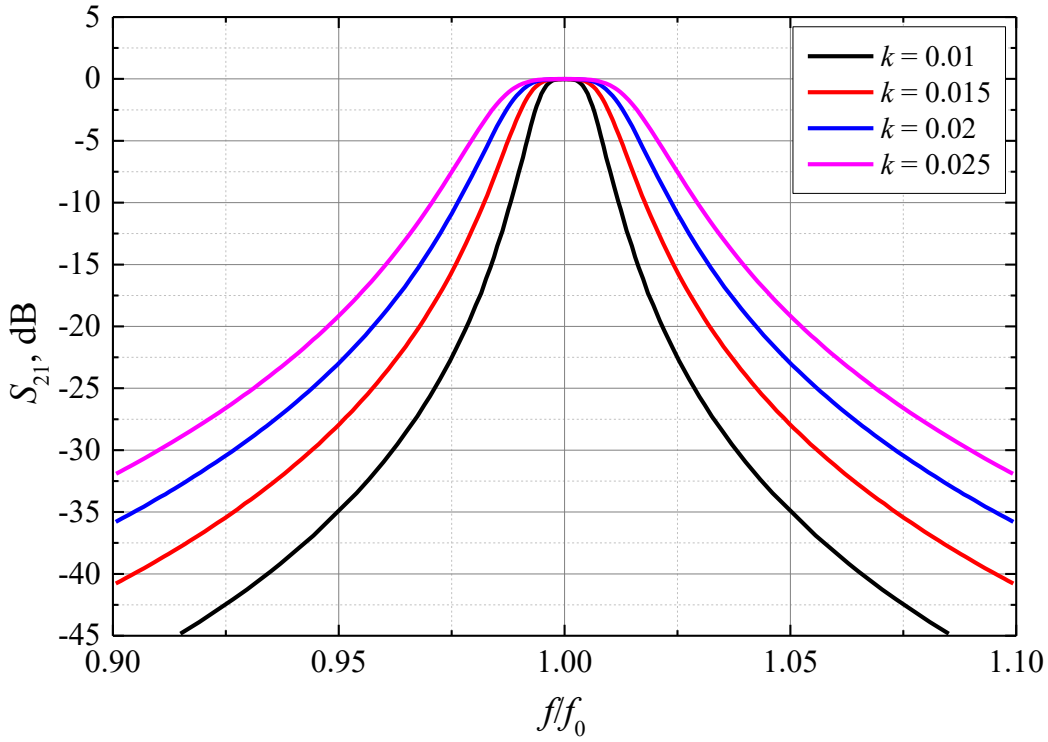


Figure 13. The frequency response of the circuit depicted in Figure 9 at various coupling coefficient values

1.3.4. Design of tunable CR filter

To achieve constant relative bandwidth, the bandwidth ($\Delta\omega$) must remain proportional to the center frequency (ω_0). Additionally, the filter's response shape should mirror the low-pass prototype, which means the normalized element values of the prototype must stay unchanged. These conditions indicate that the coupling coefficient should remain constant when the center frequency is adjusted.

Constant relative bandwidth implies that the absolute bandwidth increases linearly with the center frequency. However, increasing the bandwidth also reduces the filter's absolute cut-off rate, which is generally undesirable. These issues are avoided with constant absolute bandwidth, where the bandwidth remains fixed regardless of the center frequency.

When maintaining constant absolute bandwidth ($\Delta\omega$), the coupling coefficient is influenced by the center frequency ω_0, if the absolute bandwidth, $\Delta\omega$, is kept constant. Thus, to maintain a consistent filter response as the center frequency varies, the coupling coefficient must change inversely with the center frequency $\frac{1}{\omega_0}$.

1.4. Tuning components

From the theory discussed, it is evident that filter tunability encompasses two aspects: frequency tunability and bandwidth tunability. Achieving such tunability requires real components. Some tunable components are fabricated as MEMS structures, but on-chip tunability is primarily realized through the use of variable capacitance components.

MEMS structures offer precise mechanical adjustments to achieve tunability, providing high quality factors and low power consumption. However, for on-chip implementations, variable capacitance components, such as varactors or digitally tunable capacitors, are predominantly used. These components allow for dynamic adjustments in response to control signals, enabling the desired tuning of both frequency and bandwidth. As varactors will be implemented in this project, following section will briefly discuss the main difference between these two components.

1.4.1. Varactor diodes

Variable capacitance PN diodes, also known as varactor diodes, operate on the principle of variable depletion region capacitance. When a reverse bias is applied, the depletion region's width changes, varying the capacitance inversely with the applied voltage. The reverse bias voltage and the junction capacitance is related by [14]

$$C_j(V_r) = \frac{C_{j0}}{\left(1 + \frac{V_r}{V_{bi}}\right)^{\gamma}} \tag{29}$$

where C_{j0} is the junction capacitance at zero bias and V_{bi} is the built-in potential barrier. The exponent, γ, is dependent on the doping profile of the diode. From equation 29 it can be seen that γ determines the slope of the voltage-capacitance curve. If γ is large then a small change in voltage causes a big change in capacitance. Such varactors, which have $\gamma > 0.5$, are named hyperabrupt varactors, while an abrupt varactor has $\gamma \approx 0.5$ [15]. The ratio of minimum and maximum capacitance, C_{max}/C_{min}, of a hyperabrupt varactor can be as high as 12 [16].

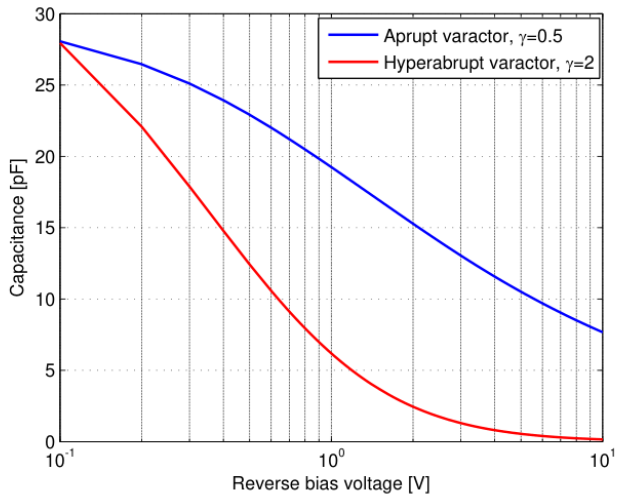


Figure 14. Typical voltage-capacitance curves for varactor diodes [15]

Varactor diodes are favored for their low cost, availability, and simple control circuits. Filters capable of tuning over relatively broad bandwidths have been developed using these diodes [17, 18]. This wide tuning capability, along with its simple control circuits, makes this technology the most attractive for this work.

1.4.2. MOS varactors

MOS varactors utilize the capacitance variation in the MOS structure, which is influenced by the voltage applied to the gate terminal. At a high gate voltage, the MOS capacitor enters the accumulation mode, resulting in high capacitance. At low gate voltage, it enters the depletion mode, leading to low capacitance. A significant benefit is the ease of integration with standard CMOS processes, which simplifies the manufacturing process and reduces costs. However, MOS varactors generally exhibit lower quality factors compared to PN diode havar varactors, which can introduce higher losses in high-frequency applications. Their tuning range is also typically narrower, and they can suffer from non-linear capacitance-voltage characteristics, which might degrade the performance in precision applications.

1.5. Literature overview

Scientific research in the development of tunable bandpass filters for the K and Q bands has seen significant advancements, driven by the growing demand for efficient and flexible satellite communication systems. These filters are essential for improving the selectivity and performance of communication channels, enabling the handling of multiple signals and frequencies. The K band (18-27 GHz) and Q band (33-50 GHz) are particularly important for satellite communications due to their high data transmission capabilities and suitability for high-frequency applications. Innovations in this field

focus on achieving tunability, low insertion loss, high selectivity, and compact design, which are critical for meeting the stringent requirements of satellite systems.

Several recent studies have contributed to the advancement of tunable bandpass filters for the K and Q bands. One notable research by Zhang et al. (2016) [19] presents a novel K-band MEMS tunable band-pass filter designed for satellite communication systems, achieving a significant tuning range of 21.69 –24.36 GHz. The filter incorporates an inductively tuned slow-wave resonator and MEMS capacitive switches, resulting in four distinct operational states with insertion losses ranging from 2.81 dB to 4.03 dB at corresponding frequencies. The actuation voltages required for these states vary between 0 and 26 V. The filter's compact size (1.56 mm x 1.46 mm) and the wide-frequency tunable range demonstrate its potential for miniaturizing millimeter-wave tunable filters while maintaining a broad tunable spectrum. The research contributes to the advancement of MEMS technology in developing smaller and more efficient tunable filters for modern communication systems. However, the presented filter does not achieve great out-of-band rejection at $f_0 \pm 25$ % and in band input return loss. The MTFB presented in this thesis will aim to achieve more competitive performance in those two regards, while also occupying smaller on-chip area and, thus, being more implementable.

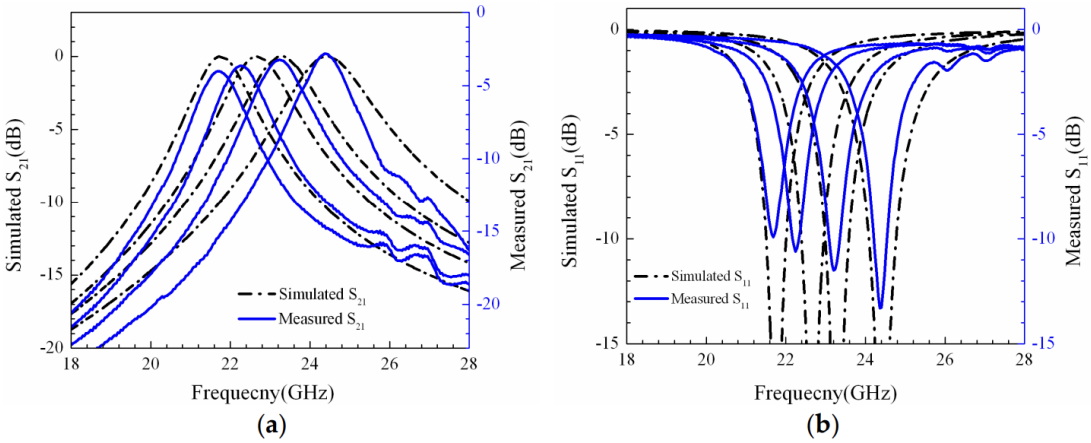


Figure 15. (a) S_{21} of measured results and simulation results; (b) S_{11} of measured results and simulation results [19]

Another notable research was conducted by Bergeras et al. [20]. The article presents two innovative MMIC architectures tunable microwave active bandpass filters, highlighting advancements in frequency tuning and bandwidth selection capabilities. The first architecture utilizes "actively coupled passive resonators" with varactor diodes for frequency tuning, exemplified by a 3-pole filter centered at 12 GHz on GaAs. The second architecture employs a channelized configuration for band selection, demonstrated by a 3-channel filter operating in the 9-15 GHz range. These designs represent a substantial

advancement in compact, low-cost, and reconfigurable solutions for RF and microwave systems, integrating filtering and amplification functions within MMIC technology. Specifically, the frequency-tunable filter exhibits a 19 % tuning capability around 11.5 GHz with a constant 10 dB gain, while the channelized filter provides bandwidth tunability from narrow (2 GHz) to wide (6 GHz).

Building on this research, the MTBF presented in this thesis will adopt the channelized principle discussed in the article, incorporating a combiner and a cascode amplifier to enhance isolation. The goal is to achieve a more competitive return loss and to operate at a higher working frequency, while maintaining the same 2 GHz bandwidth, which presents additional challenges at Q band frequencies. Additionally, the project aims to reduce the overall on-chip area by using fewer filter banks and smaller components.

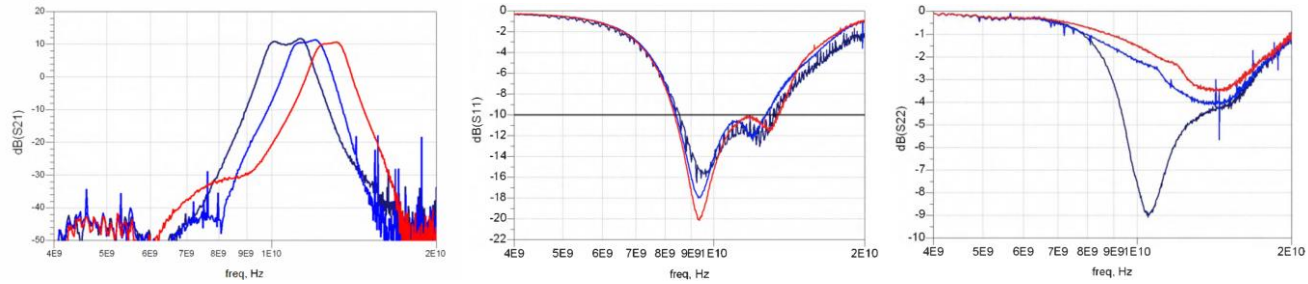


Figure 16. Measurement results of tunable filter [20]

The third example is a 20 GHz varactor-tuned MMIC filter presented in 2005 by Fan et al. [21]. The structure of the filter is shown in Figure 15, where the radial stubs are replaced with varactors for the tunable version. The schematic of the negative resistance (Figure 17) features a common-gate transistor that presents an almost constant reactive part and a negative resistance in the band of interest. A photograph of the chip, along with the simulated and measured S-parameters, is shown in Figure 16. The selectivity and tunability (17.5–21.5 GHz) are very good, but the passband flatness is poor (approximately 6 dB), and the gain variation with tuning is significant (from −11 dB to a few dB). The bandwidth is about 900 MHz, centered at 22.6 GHz, with the input return loss better than 8 dB across the passband. The noise figure is 17.5 dB, and the compression point is −20 dBm. The total reported chip area is 1 mm², and the power consumption is 50 mW.

Compared to this research, the MTBF will aim to have better passband flatness and significantly reduced amplitude variation with tuning voltage. Additionally, the on-chip area should be similar, with the MTBF in this work incorporating both K and Q band filters. Finally, the power consumption in both designs should be comparable.

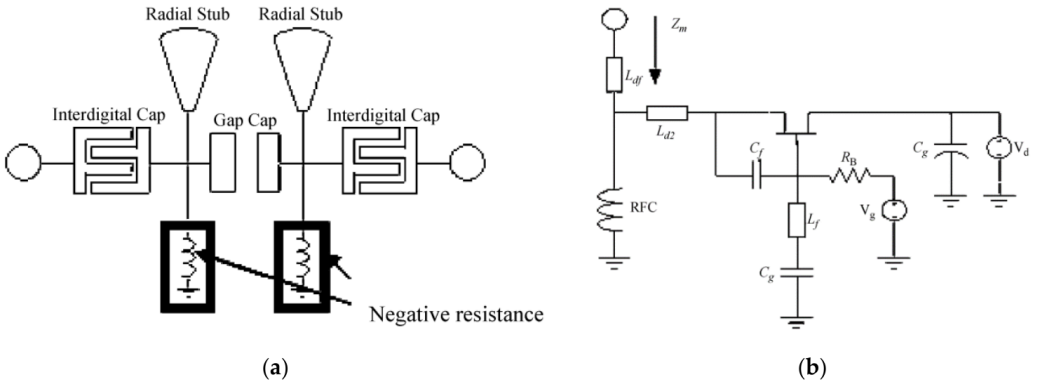


Figure 17. (a) The structure of the filter and (b) the schematic of the negative-resistance component from [21]

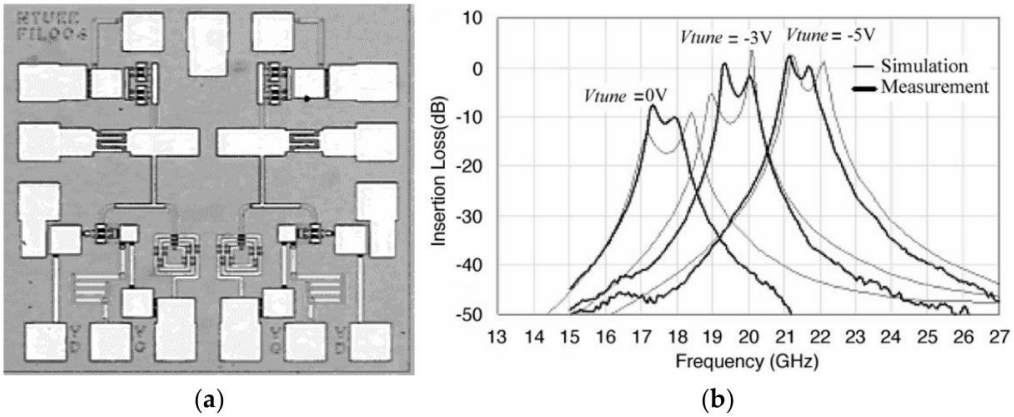


Figure 18. (a) Chip photograph and (b) measured and simulated S-parameters of the tunable filter [21].

Research on tunable bandpass filters operating in the Q-band (33-50 GHz) is limited due to technical challenges and the need for advanced materials [22]. However, a notable contribution in this field is the paper "A 42.5–51.0 GHz SiGe BiCMOS Integrated Tunable Bandpass Filter and Attenuator" by Moradinia et al. [23]. This work addresses two key challenges at the Q-band receiver side: preventing saturation of the receiver baseband amplifiers and digitizer due to high input power levels, and maximizing the spurious-free dynamic range (SFDR) by avoiding unwanted tones mixing into the baseband. The paper introduces a device termed the "filttenuator," which combines a tunable bandpass filter with a digital step attenuator, implemented using 130 nm SiGe BiCMOS technology. The filttenuator features a center frequency tunable from 44.5–49.0 GHz with a constant 3 dB bandwidth of 4 GHz, covering an overall frequency range of 42.5–51.0 GHz. It achieves stopband-to-passband rejections between 38 dB and 58 dB and exhibits a sharp roll-off of 66 dB/octave.

The loss compensation amplifier is implemented in this work in a form of a single-stage cascode with L-match input and output networks. Transistor sizing was set to maximize gain while conserving power. Input and output networks match the cascode device terminals to 50 Ω over 42–51 GHz. A 25 Ω de-Q'ing resistor in series with the shunt peaking inductor ensures wideband output matching and high gain. The amplifier, biased for maximum gain with power efficiency, achieves 16 dB peak gain at 47 GHz, a 3 dB bandwidth from 41.5–53.0 GHz, and consumes 25 mW from a 2.5 V supply. The shematic of TBF and loss compensation amplifier are shown in Figure 19.

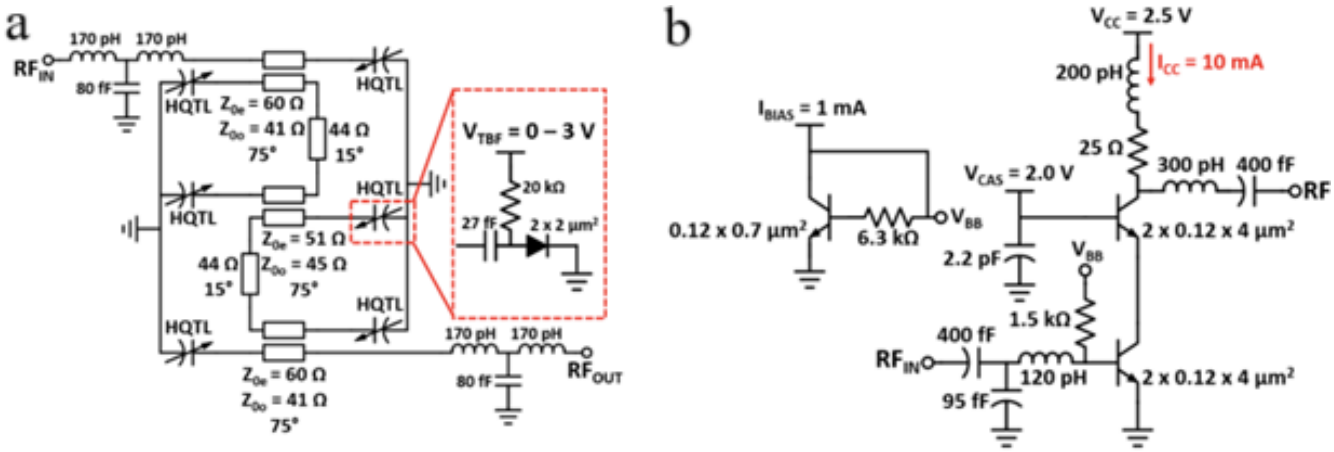


Figure 19. (a) Circuit schematic of the designed TBF will all electrical lengths at 50 GHz and (b) Circuit schematic of the designed loss compensation amplifier. [23]

Building on this research, the MTFB proposed in this thesis aims to achieve tunability over a similar frequency range but with a significantly smaller IBW of 2 GHz, a challenging goal at such high frequencies. The out-of-band rejection will be comparable to that reported in Moradinia et al.'s work (Figure 20). Additionally, the MTFB will utilize a similar loss-compensating amplifier architecture to mitigate high Q-band losses. The proposed MTFB design promises a more competitive on-chip area, occupying less than 1 mm² compared to the 2.3 mm² of the active filttenuator area in the referenced study, while covering both K and Q bands instead of just one.

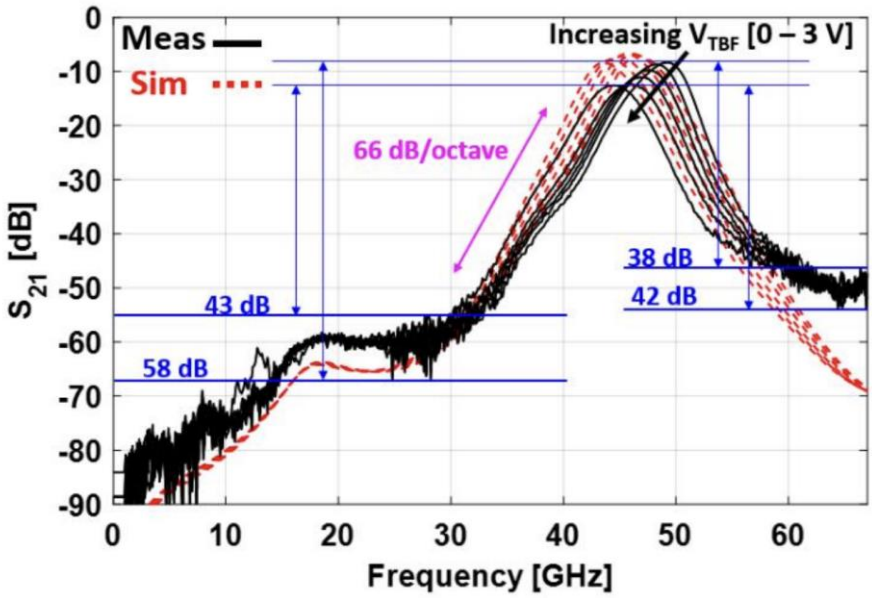


Figure 20. Measured vs. simulated performance of the filttenuator from DC – 67 GHz showing all filter states for a fixed reference attenuation state, steep roll-off and worst-case, best-case stopband to passband rejections [23].

Concluding the literature overview, the proposed MTBF aims to achieve similar insertion losses to those presented in the articles while maintaining competitive out-of-band rejection (< 30 dBc) and high tunability. The MTBF presented in this thesis will utilize a highly integrable on-chip design, allowing it to be incorporated into a full receiver front-end chip, unlike some articles that employ MEMS components which are impossible to integrate on-chip. The MTBF will also strive for the most compact on-chip area among all works presented, maintaining a narrow 2 GHz bandwidth, which presents additional challenges at Q band frequencies. Furthermore, it will feature a loss-compensating amplifier architecture to mitigate high K and Q-band losses, ensuring competitive input return loss. Overall, the MTBF will balance tunability, performance, and integration, positioning itself as a robust solution for modern high-frequency applications.

2. Technical part

2.1. Project objectives and specifications

The aim of this thesis is to design and develop a Multiband Tunable Bandpass Filter (MTBF) for the K and Q bands. To make it a competitive component for LEO satellites, it will need to meet a significant number of requirements. The following sections will explain in detail the physical meaning of each requirement set for the project and the target values to be achieved.

2.1.1. Center frequency

The center frequency of a bandpass filter is defined as either the geometric or arithmetic mean of its upper and lower cutoff frequencies, also known as the 3 dB points. In the example shown in illustration below, the center frequency is denoted by f_0. For this project, the center frequency will be tunable across two specific ranges: from around 17 GHz to about 21.5 GHz within the K band, and from about 37 GHz to about 43 GHz within the Q band. These frequency ranges have been selected as they cover the emerging satellite datalink bands [24].

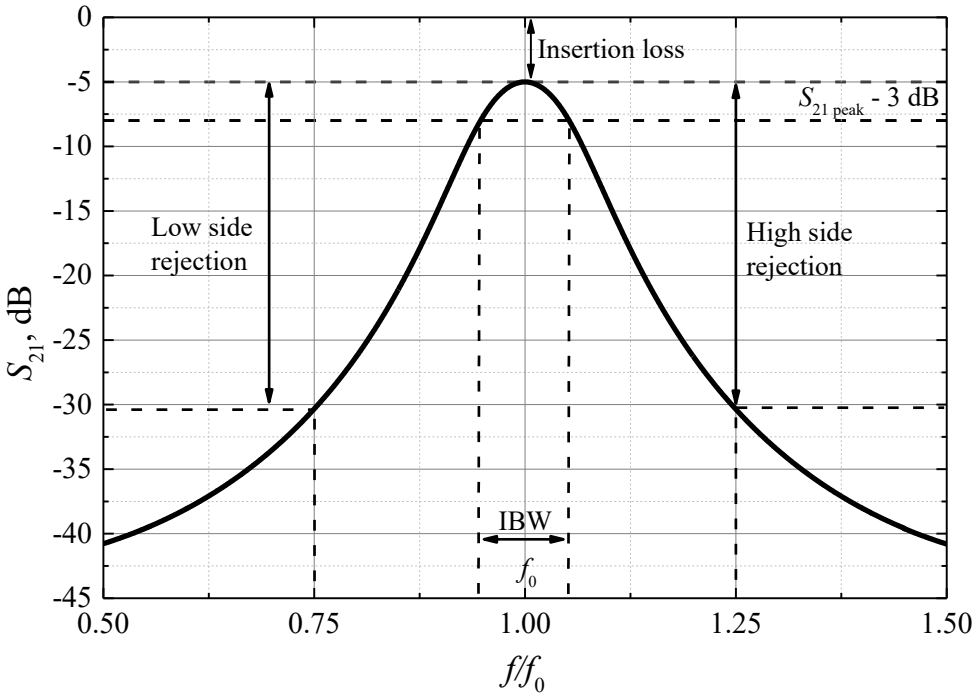


Figure 21. An example of filter amplitude response and related parameters

2.1.2. Instantaneous bandwidth

Bandwidth refers to the width of the passband of a bandpass filter and is defined as the frequency difference between its lower and upper 3 dB points. Additionally, the relative or fractional bandwidth of the filter is considered, which is the ratio of the filter's bandwidth to its center frequency.

In this project, the tunable 3 dB bandpass bandwidth will be less than 11.8% (under 2 GHz) in the K band, and less than 5.3% (under 2 GHz) in the Q band. Maintaining a narrow 3 dB bandpass bandwidth is crucial as it enhances the signal-to-noise ratio (SNR), minimizes interference, and effectively filters out unwanted harmonic signals.

2.1.3. Insertion loss

Insertion loss is the ratio of a signal level in a test configuration without a filter present ($|V_1|$) to that when the filter is present ($|V_2|$) and is calculated as shown in the equation below.

$$IL = 20\log_{10}\frac{|V_1|}{|V_2|}[\text{dB}] \tag{30}$$

It is important to note that insertion loss should be considered a critical specification for both the transmission (Tx) and reception (Rx) sides. On the Tx side, insertion loss is a significant factor because power efficiency is a major system cost driver. On the Rx side, insertion loss affects the overall noise figure of the receiver, impacting its performance. In this thesis, the goal is to maintain insertion loss below 10 dB. This specification aligns with current state-of-the-art (SotA) solutions.

2.1.4. Out-of-band rejection

A bandpass filter must prevent interference from signals outside the desired bandwidth. Therefore, the filter needs the capability to reject (attenuate) out-of-band emissions. These emissions, although far from the band of interest, can still interfere with the signals within the passband through effects such as aliasing.

In this project, out-of-band isolation will be defined as the difference in signal levels at the center frequency f_0 and f_0 ± 25 %. This isolation should be better than 30 dBc. Ensuring that out-of-band isolation remains as high as possible will maximize suppression of out-of-band interference, thereby enhancing the filter's performance and reliability.

2.1.5. Return loss

As discussed in the previous section on scattering parameters, there is always some power loss when power is applied to the device under test due to imperfect port matching. These losses occur at both the input and output ports of the device. In this project, return loss is defined as the maximum value of

the S_{11} or S_{22} parameter in band and shall be less than 12 dB. This specification is set to ensure that the MTBF maintains sufficiently wideband matching, thereby enhancing the overall reliability and performance of the device.

2.1.6. Linearity

A linearity expressed as Input 3rd Order Intercept Point (IIP3) of at least 10 dBm is required to avoid signal compression in MTBF. Linearity refers to the upper operational limit of an amplifier (or any device) under a high signal condition, until signal compression or third-order intermodulation products start to interfere with signal amplification or reduce the sensitivity of weak signal reception. Perfect linearity would mean that the output is always proportional to the input. Two key parameters are often used to assess linearity: the 1 dB compression point and the third-order intercept point. The hypothetical third-order intercept point is a commonly used method for evaluating the linearity of a device. This concept arises from a situation where two closely spaced tones ω_1 and ω_2 are present at the input port:

$$v_i = V_0(cos\omega_1 t + cos\omega_2 t) \tag{31}$$

where v_i is the time-varying input voltage, V_0 is the initial signal amplitude. The given expression (31) can be expanded by the Taylor series:

$$\begin{aligned} v_0 = {} & a_0 + a_1 V_0(cos\omega_1 t + cos\omega_2 t) + a_2 V_0^2(cos\omega_1 t + cos\omega_2 t)^2 + a_3 V_0^3(cos\omega_1 t + cos\omega_2 t)^3 + \cdots \\ & = a_0 + a_1 V_0 cos\omega_1 t + a_1 V_0 cos\omega_2 t + \frac{1}{2} a_2 V_0^2(1 + cos2\omega_1 t) + \frac{1}{2} a_2 V_0^2(1 + cos2\omega_2 t) \\ & + a_2 V_0^2 cos(\omega_1 - \omega_1)t + a_2 V_0^2 cos(\omega_1 + \omega_1)t + a_3 V_0^3(\frac{3}{4} cos\omega_1 t + \frac{1}{4} cos3\omega_1 t) \\ & + a_3 V_0^3(\frac{3}{4} cos\omega_2 t + \frac{1}{4} cos3\omega_2 t) \\ & + a_3 V_0^3\left[\frac{3}{2} cos\omega_2 t + \frac{3}{4}\cos(2\omega_1 - \omega_2)t + \frac{3}{4}\cos(2\omega_1 + \omega_2)t\right] \\ & + a_3 V_0^3\left[\frac{3}{2} cos\omega_1 t + \frac{3}{4}\cos(2\omega_1 - \omega_2)t + \frac{3}{4}\cos(2\omega_1 - \omega_2)t\right], \end{aligned} \tag{32}$$

From equation (32), the following observation can be made: the third-order product increases as the cube of the initial amplitude (V_0^3). Third-order products are defined as frequency components consisting of three ω_1 or ω_2 terms in a certain combination, e.g., $(2\omega_1 \pm \omega_2)t$ or $3\omega_1 t$. For small amplitude input signals, this will not be an issue, but as the input power increases, the power of the third-order products will increase rapidly. As shown in Figure 22, the third-order intercept point is the point where the cubic third-order product (n = 3) surpasses the linear response (n = 1). Although, as mentioned,

this point is purely hypothetical and uses theoretical linear curves, in practice, both the third-order product and the linear response compress earlier [10].

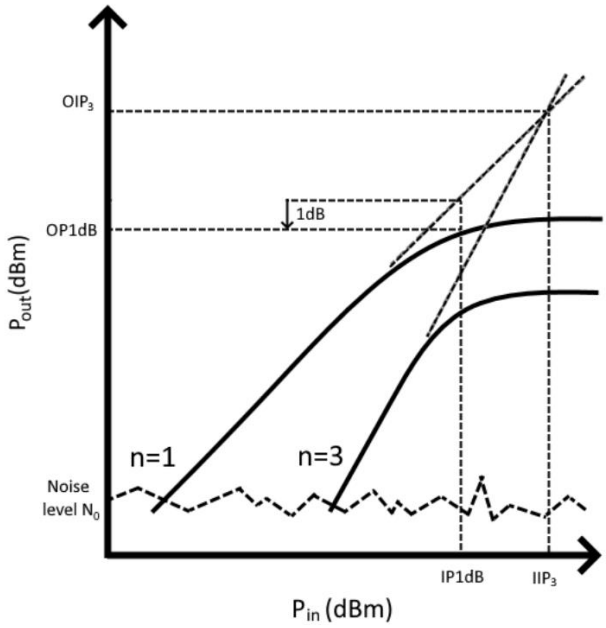


Figure 22. Depiction of first-order (n = 1) and third-order (n = 3) input signal saturation [7]

The 1 dB compression point (OP1dB) is a complementary parameter to the third-order intercept point (IIP3). OP1dB defines the input power level at which the gain of an amplifier or system decreases by 1 dB from its small-signal gain, indicating the onset of significant non-linear behavior. The 1 dB compression point is typically about 10 dB lower than the Input Third-Order Intercept Point (IIP3). As illustrated in Figure 22, the linear characteristic ceases to be ideal at a certain input power level, where the system's response becomes nonlinear and distortions appear in the output signal form.

2.1.7. Total area

As stated previously, the main motivation to develop MTBF MMIC is its capability to be integrated thus saving precious satellite PCB area and reducing cost. The MMIC developed during this project MMIC shall occupy a total area of $< 1\ mm^2$ as miniaturized and cost-effective design is required for use in satellite systems. The main challenge is expected to arise from multiple inductors within the MMIC. The problem might be mitigated by using topologies with less inductors or selecting inductors with smaller area and thus sacrificing some of their quality.

2.1.8. Supply voltage and current

Due to the active nature of the filter, it will inevitably consume some power. The requirements for voltage and current are derived from the existing device with which the MTBF will need to work in

conjunction. This means that the power consumption of the filter must be compatible with the power supply specifications and limitations of the existing system. Ensuring this compatibility is crucial for maintaining overall system performance and reliability. In this project, supply current should stay below 40 mA and supply voltage range should be 3.0 – 3.6 V.

2.1.9. Group delay

Group delay is a critical parameter for RF filters because it quantifies the time delay experienced by various frequency components of a signal as they pass through the filter. A consistent group delay ensures minimal distortion and phase shift, preserving the waveform's shape and maintaining the integrity of the transmitted information. Variations in group delay can lead to signal degradation, causing issues such as data errors and reduced performance in high-frequency applications. Therefore, achieving a flat group delay response is essential for optimizing the performance and reliability of RF systems. In this project, the targeted group delay will be < 1 ns.

2.2. Summary of technical parameters

The complete list of targeted specifications in this project is listed in the Table 1.

Table 1. List of MTBF targeted specifications

No.	Req.	Value
Reqmt. 1	Frequency range	About 17 GHz to 21.5 GHz in K band and about 37 GHz to 43 GHz in Q band
Reqmt. 2	Tunable 3 dB bandpass bandwidth	Less than 11.8 % (< 2 GHz) at the K band. Less than 5.3 % (< 2 GHz) at the Q band.
Reqmt. 3	Insertion loss	Better than 10 dB
Reqmt. 4	Return loss	Less than 12 dB
Reqmt. 5	IIP3	Better than 10 dBm
Reqmt. 6	Out-of-band isolation	Better than 30 dB at fc ± 25 %
Reqmt. 7	Total area	< 1 mm^2.
Reqmt. 8	Max. supply current	40 mA

Reqmt. 9	Control voltage range	-2.6 V to 2.6 V
Reqmt. 10	1dB compression point	> 0 dBm
Reqmt. 11	Group delay	< 1 ns
Reqmt. 12	Isolation of switched-off filters	< -40 dB

2.3.Implementation

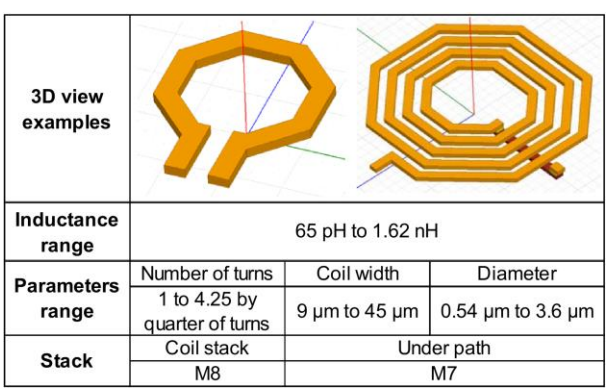
The proposed MTBF will employ the channelization principle, meaning it will be split into two channels for each band, with the center frequency of each channel being tunable. The working procedure will be as follows: when a new center frequency is requested, voltage will be supplied to the pin responsible for turning on and off a specific channel. At the same time, any other voltage, if present, should be turned off. Using the filter tuning voltage, the center frequency is fine-tuned to the desired one. When a new center frequency is requested, the process is repeated.

3. Experimental part

3.1. Technology

The technology chosen for this project is the 55 nm SiGe BiCMOS process developed by STMicroelectronics [25]. This technology features a SiGe HBT based on a conventional double-polysilicon self-aligned (DPSA) architecture, with emitter-base self-alignment provided by Selective Epitaxial Growth (SEG) of the SiGe:C base. Three collector flavors, leading to different f_T/BV_{CEO} trade-offs for the High Speed (HS), Medium Voltage (MV), and High Voltage (HV) HBTs, are available. The technology includes a back-end of line (BEOL) featuring eight copper metal layers and one aluminum capping layer. This BEOL is fully compatible with existing 55 nm CMOS libraries and provides enhanced performance for millimeter-wave passives. Varactors, inductors, and transmission lines have been specifically designed for millimeter-wave applications.

The 55 nm SiGe BiCMOS technology is expected to be highly beneficial for this project for several key reasons. First, the technology offers several SiGe HBT flavors, each with specific current gain transit frequency and maximum oscillation frequency (f_T, f_{MAX}). The HS, MV, and HV transistors provide frequencies of (325, 375) GHz, (180, 385) GHz, and (65, 270) GHz, respectively, with BV_{CEO} values of 1.5 V, 1.9 V and 3.2 V [25]. These options will be advantageous for the amplifier design integrated with the filters. Secondly, 55nm BiCMOS technology has hyper-abrupt junction varactors, which offer favorable characteristics for MTBF compared to NMOS varactors. Thirdly, the technology provides an option for mmWave inductors with two distinct geometries (Figure 23). One of these geometries occupies a very small area, enabling high compactness and compliance with Reqrm. 7, ensuring the total chip area remains under 1 mm^2.



Inductance range	65 pH to 1.62 nH		
Parameters range	Number of turns	Coil width	Diameter
	1 to 4.25 by quarter of turns	9 µm to 45 µm	0.54 µm to 3.6 µm
Stack	Coil stack	Under path	
	M8	M7	

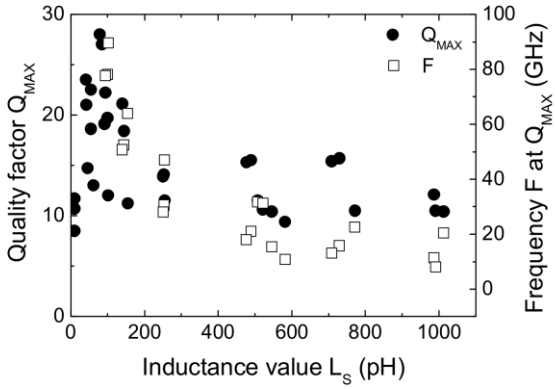


Figure 23. Inductors available in the selected technology for this project [25]

3.2.Schematic design

At the beginning of this project, various filter design architectures were tested and compared. The report in the following section presents some of the most promising candidates and provides a general overview of their performance.

3.2.1. The MTFB candidate architecture analysis

There are several different *LC* component-based architectures, all of which are based on coupled resonators. The main differences arise from the type of resonator selected (series or parallel) and the type of coupling ("T" or "π"). These choices result in slightly different characteristics. The main trade-offs had to be considered to select the most fitting architecture. The final choice of the architecture was made out of three main candidate which will be presented in the following sections.

3.2.1.1. Direct-Coupled Series Inductor design

The Direct-Coupled Series Inductor design, shown in Figure 24, involves shunt parallel resonant *LC* circuits linked together through series inductors. This approach is beneficial when capacitive elements cause more losses than inductors or offer less favorable trade-offs. As can be seen in Figure 24, due to a bigger number of inductors used, the majority of energy is stored magnetically. This architecture excels at isolating higher frequencies, as inductors connected in series block high frequency signal. Despite its advantages, it is generally considered impractical due to the high number of inductors needed (e.g., it uses 7 inductors for 3rd order designs compared to 3 inductors in other designs). Inductors take up much more space than other components, posing challenges in keeping the total chip area under 1 mm^2.

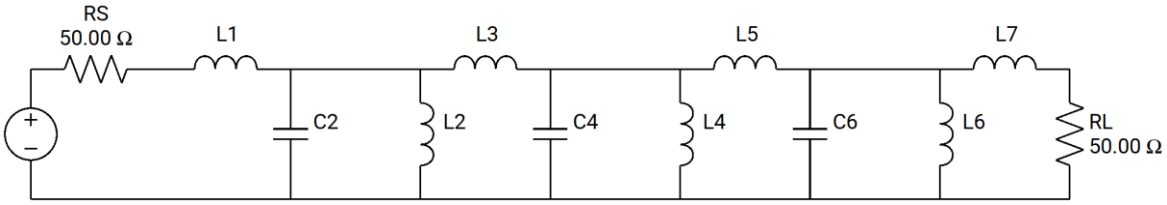


Figure 24. Direct-Coupled Series Inductor topology [26]

3.2.1.2. Chebyshev Direct-Coupled Series Capacitor design

Direct-Coupled Series Capacitor design, illustrated in Figure 25, consists of shunt parallel resonant *LC* circuits connected by series capacitors. This design is beneficial when custom inductors are needed, as all inductors ideally have the same inductance values. It is particularly effective at isolating lower frequencies as in series connected capacitors in conjunction with shunt inductors works as RF open and RF short to ground respectively. The main drawback of the design comes from susceptibility to

process variation, as relatively small changes in inductor value can cause signal leakage. Finally, although not shown here, the varactors used for frequency tuning would have to be biased with constant DC voltage. Each of the shunt inductors would need a subsequent DC blocking capacitor, which would add unnecessary complications.

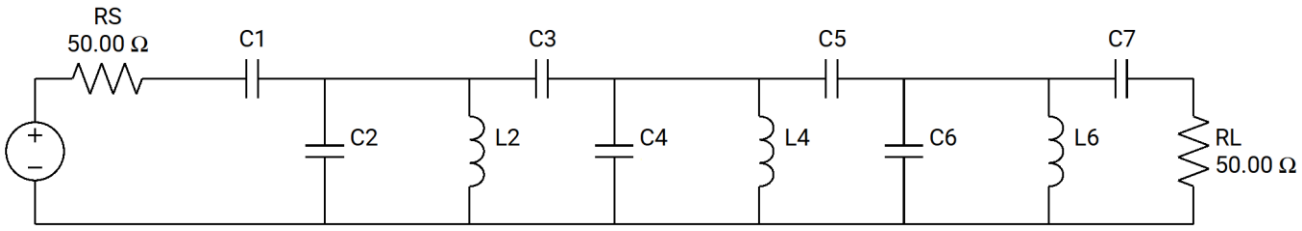


Figure 25. Direct-Coupled Series Capacitor topology [26]

3.2.1.3. Tubular design

The tubular bandpass filter architecture is a variation of the direct-coupled shunt capacitor bandpass filter, achieved by transforming internal capacitor "T" networks into equivalent "π" networks. This design is beneficial when the filter's center frequency is adjusted solely by capacitive elements. It is particularly effective at isolating higher frequencies. This architecture is excellent for fine-tuning filter characteristics in both schematic and layout views due to the number of components involved. However, it often compromises insertion loss for this flexibility. Despite this trade-off, the architecture was chosen as the best option for implementing the MTFB, as it provided superior performance characteristics when tunability was considered. Furthermore, the drawback of having more components was minor because the combined on-chip area of capacitors and varactors was significantly smaller than that of inductors.

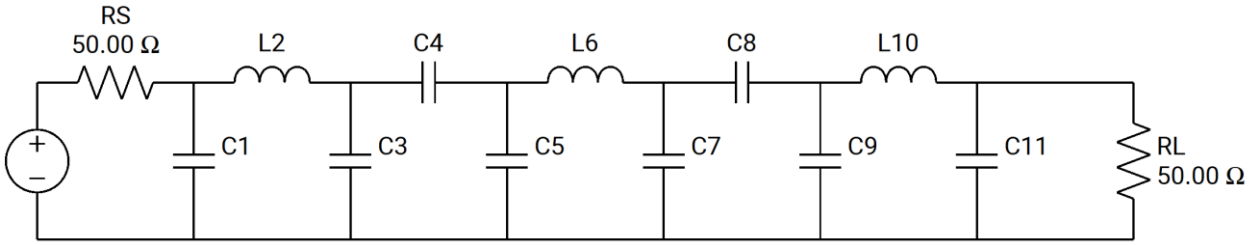


Figure 26. Tubular bandpass filter topology [26]

3.3.Filter bank schematic design in K-band

The design procedure of a bandpass filter begins with establishing an ideal case. The goal at this stage is to evaluate the theoretical performance and determine the required component values. This preliminary evaluation helps to determine the feasibility of implementing these components into the actual design. With the help of online filter design tool [26], ideal 4^{th} order filter design was created and

its main performance metrics were tested. The schematic with specific component values can be seen in Figure 27.

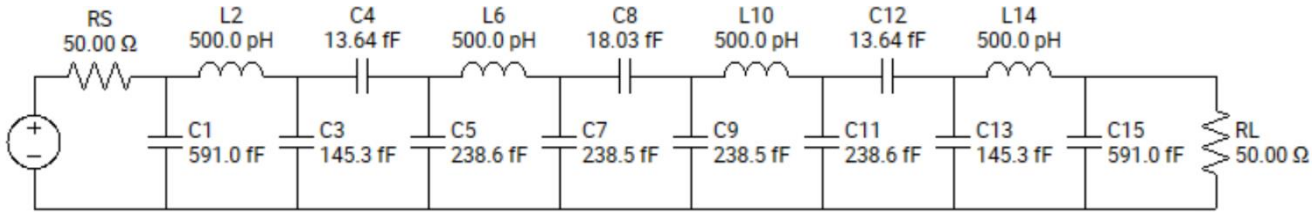


Figure 27. 4th order tubular filter design with ideal components [26]

The corresponding *S*-parameter response is shown in Figure 28. Due to the fact that the components are ideal, the filter response has 0 dB insertion loss and exhibits three clearly visible return loss minima, resulting from the 4th order configuration. Additionally, the filter topology is fully symmetrical, with the symmetry axis passing through the center capacitor, C8. This symmetry reduces the complexity of implementing real components, as they can be matched and optimized together. Consequently, the S_{11} and S_{22} responses are identical. This ensures minimized return losses on the input side and a linear connection with the amplifier on the output side, meaning the S_{21} responses will add linearly without introducing additional losses.

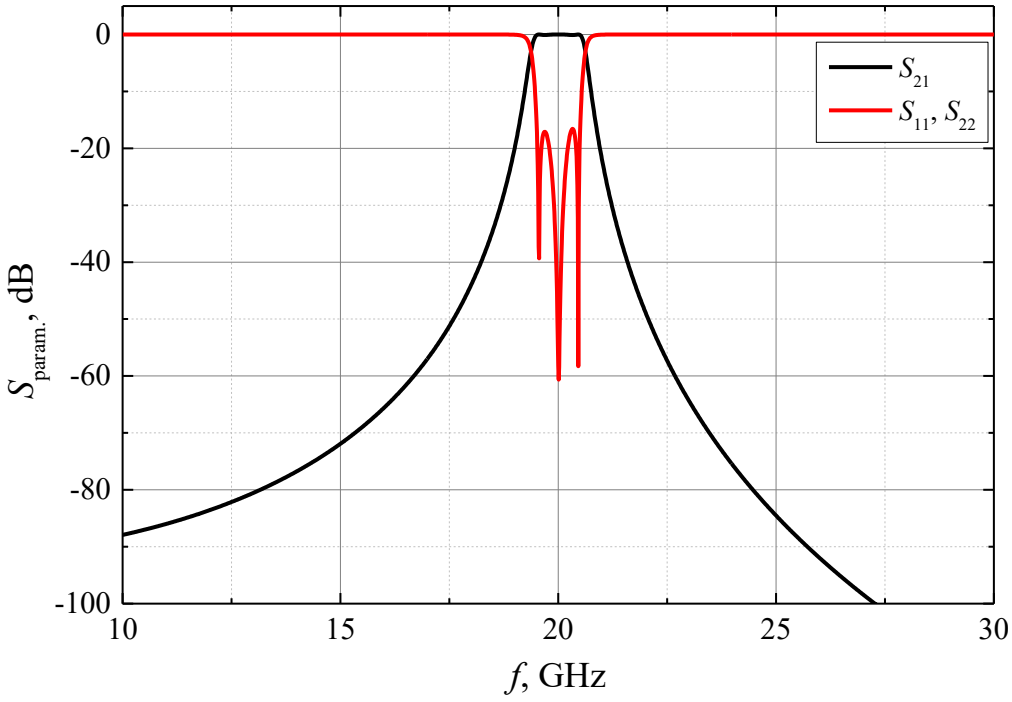


Figure 28. *S*-parameter response of an ideal 4th order tubular Chebyshev filter with 0.1 dB ripple

At this stage, an investigation into the feasibility of achieving component values using on-chip parameterized cells (Pcells) provided in the PDK was necessary. The study began with testing the option of on-chip inductors, focusing on their main trade-offs. Two types of inductors were evaluated: one designed for high-frequency operation and another optimized for significantly higher quality.

The results of this evaluation are illustrated in Figure 29, which shows two exemplary inductors, each designed to have an inductance value of 300 pH at the K-band. The high-frequency inductor demonstrated improved performance in terms of frequency response but at the cost of lower quality factor. Conversely, the high-quality inductor exhibited superior quality factors but was less effective at high frequencies and required significantly more on-chip area.

Given the stringent requirement for a small total on-chip area for the MTFB proposed in this work, the smaller high-frequency inductor was selected, despite its lower quality factor. This decision, unfortunately, led to reduced filter performance. These findings highlight the critical balance between frequency performance and quality factor in the design of on-chip inductors.

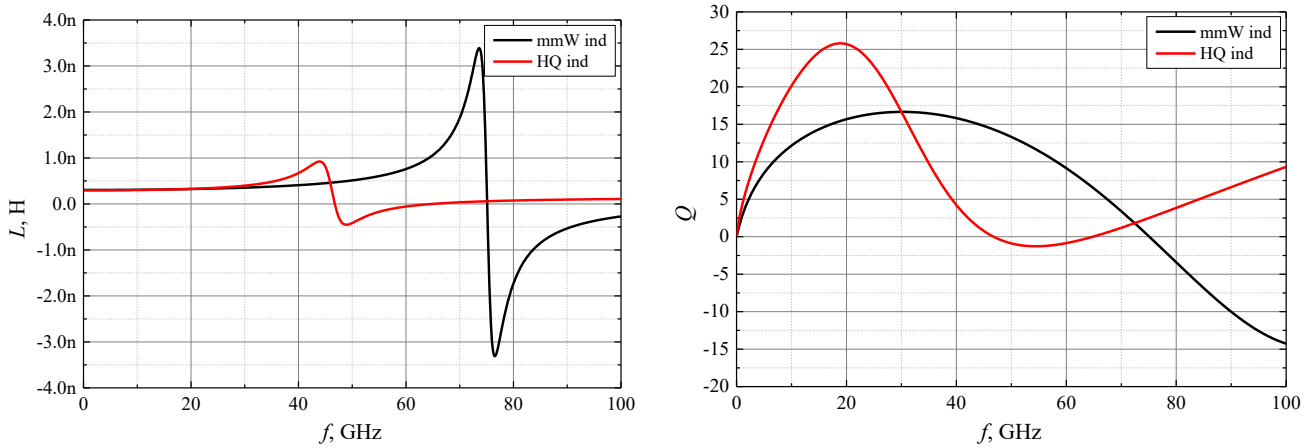


Figure 29.(a) Inductor inductance dependency on frequency and (b) inductor quality dependency on frequency

Following the analysis of the inductors, testing of another on chip component: the capacitors, was performed. The capacitors selected for this project were metal-oxide-metal (MOM) capacitors fabricated using the back-end-of-line (BEOL) interconnect layers of BiCMOS technology. An exemplary structure of such a capacitor is shown in Figure 30.

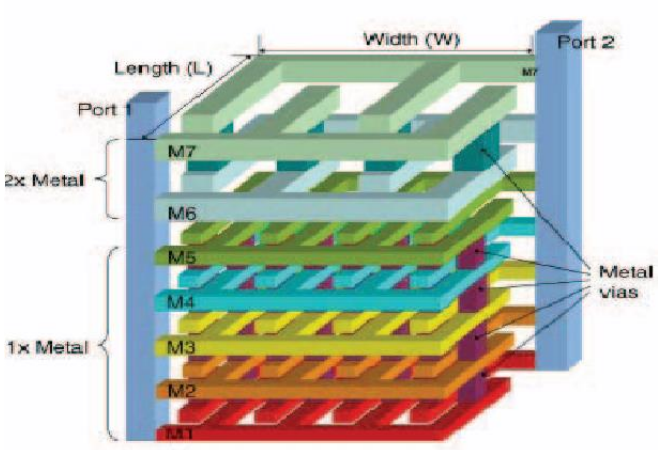


Figure 30. Illustration of a capacitor made from BEOL metals available in the technology [27].

These capacitors are widely used in advanced BiCMOS technologies due to their lower manufacturing costs and high capacitance density compared to thin-film metal-insulator-metal (MIM) and MOS capacitors [28, 29]. In this project, the capacitors served multiple purposes: they were used for isolating RF and DC components, as part of resonators in filters, and as components of *LC* matching networks between separate MMIC stages.

The investigation of MOM capacitors in the technology used for this project demonstrated that it was possible to achieve the required capacitance values while maintaining a significantly high quality. Similar to inductors, the quality factor of the capacitors is directly related to the area they occupy, as illustrated in Figure 31. It was observed that by using more layers for the capacitor, it was possible to achieve the same capacitance over a smaller area, though this approach reduced the quality factor.

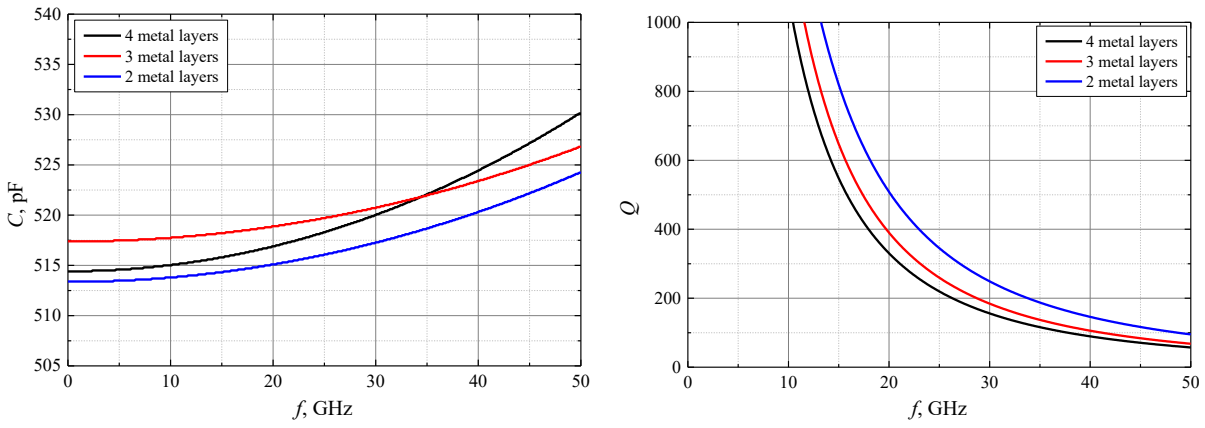


Figure 31. Capacitance and quality of MOM capacitors available in the technology as a function of frequency as the number of metals in the capacitor varies

However, due to the fact that capacitors are generally much smaller than inductors, opting for a higher quality factor at the expense of occupying a larger area was deemed preferable. This decision allowed for improved filter bank performance in terms of insertion loss and out out-of-band rejection without significantly impacting the overall chip area. Thus, the capacitors selected for this project effectively balanced the need for high performance with the constraints on available space.

The final component of the filter bank is the varactor, which facilitates tunability across the frequency range. The technology employed provides hyper-abrupt varactors, which are preferred over MOS varactors for several reasons. Although the achievable capacitance values are sufficiently high for the application, the resulting quality factor (Q) is suboptimal. Figure 32 illustrates the dependence of capacitance and quality on the tuning voltage, showing that typical quality values in the K band range between 10 and 15. This reduction in resonator quality impacts the overall performance of the filter bank. Consequently, there is a compromise between tuning range and other filter parameters, such as insertion loss, instantaneous bandwidth (IBW), and out-of-band rejection. This compromise can be mitigated by adding higher-quality capacitors in parallel. While this approach reduces the tuning range and necessitates the use of more filter banks, it enhances the performance of each individual filter bank.

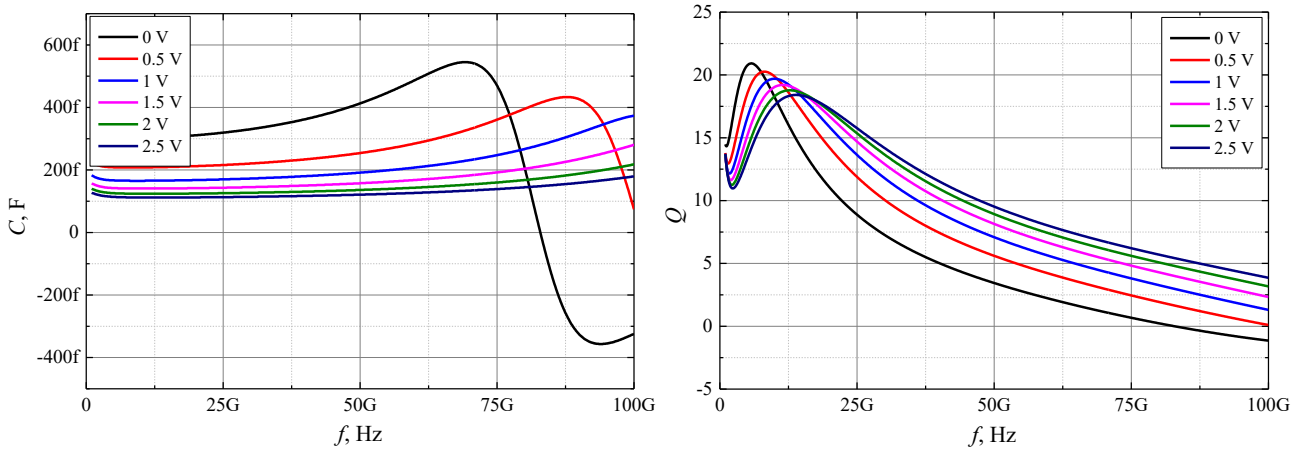


Figure 32. Capacitance and quality of hyper abrupt varactors available in the technology as a function of frequency as the tuning voltage varies

The final filter bank schematic is provided in Figure 33. The topology used is a 4th order tubular filter. As discussed earlier, the capacitors offer substantially higher quality but lack tunability. To achieve a balance between high quality and tunability, the capacitors are connected in parallel with varactors. In this way, capacitors constitute the majority of the capacitance in the resonators, thereby contributing significantly to the overall higher quality of the filter bank. This allows each varactor to be smaller, resulting in reduced tunability but enhanced performance.

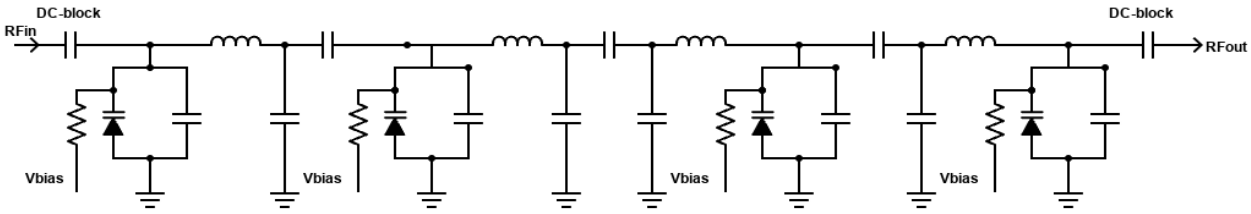


Figure 33. Final architecture of K-band filter bank

The varactors are biased through high-value resistors (> 100 kΩ), which create the necessary voltage on the varactors' cathodes without providing a direct path for the RF signal to ground. During optimization, it was observed that some varactors reached their minimal capacitance values, and these varactors were subsequently removed from certain resonators in the filter bank to improve performance.

Additionally, DC blocks are placed at both the input and output of the filter to block any DC components, ensuring that only the desired RF signals pass through. This configuration allows the filter bank to achieve a high-quality performance with the necessary tunability while maintaining the integrity of the RF signal path.

3.4. Amplifier design in K band

3.4.1. Topology

The first step in designing a high-frequency amplifier is selecting the appropriate amplifier topology. The most common amplifier topologies used at mm-wave frequencies are illustrated in Figure 34. Compared to single-transistor topologies, the cascode amplifier shown in Figure 34(c) consists of a common-emitter (CE) stage (Q1) connected to a common-base (CB) stage (Q2). The advantages of this topology over the other two include a significant increase in voltage gain compared to a CE amplifier and the suppression of the Miller effect, which results in increased bandwidth. The cascode topology, operating at frequencies significantly lower than the transistor's maximum frequency, low noise figure (NF) due to increased gain, and excellent reverse isolation (S12). This is due to the reduced direct coupling between the input and output in the cascode configuration compared to the CE topology.

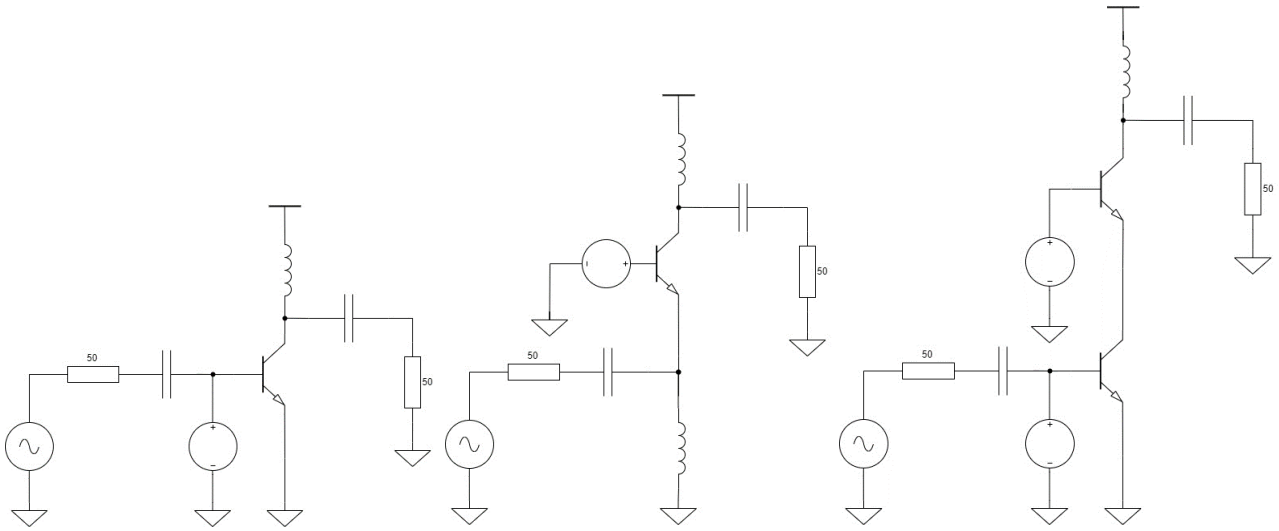


Figure 34 Several popular amplifier topologies: (a) CE stage, (b) CB stage, (c) cascode amplifier.

This characteristic is crucial for this project, as filter blocks interconnected with splitters require good reverse isolation to minimize undesired signal leakage and interference between different filters or channels within the block. Finally, the cascode topology provides a higher 1 dB compression point. Given these advantages, the cascode topology was selected for this project over the other single-transistor topologies.

3.4.2. DC Biasing and Transistor Sizing

In this project, the amplifiers operate at frequencies significantly lower than the transistors' f_T, making *NF* and maximum operating frequency optimization less critical. Instead, achieving a high output power compression point and good linear gain were prioritized.

For optimal performance of the cascode amplifier, both the common-emitter (CE) and common-base (CB) stages must be properly biased to ensure that both transistors operate in saturation. This configuration requires a supply voltage higher than the breakdown voltage of a single transistor, as the voltage at the emitter of the CE transistor (Q1) will be lower than the supply voltage due to the voltage drop across the CB transistor (Q2).

The final amplifier schematic is illustrated in Figure 35. The loss compensation amplifier is implemented as a single-stage cascode with *L*-match networks for input and output matching. DC biasing is achieved using a three-resistor voltage divider configuration. A large capacitor is connected to the base terminal of Q2 to create an AC short to ground. Additionally, a small inductor is connected to the emitter of Q1 to improve linearity through inductive emitter degeneration and input matching by compensating some of the input capacitance.

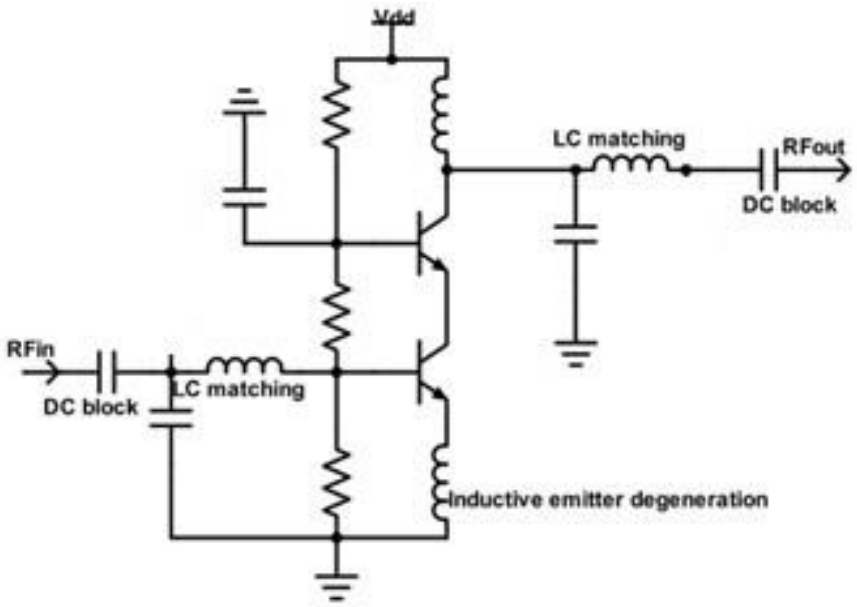


Figure 35. K band amplifier schematic

Emitter degeneration improves linearity by introducing local negative feedback, which stabilizes the operating point of the transistor and reduces the gain variations due to changes in the input signal amplitude. This feedback mechanism linearizes the transfer characteristic of the transistor, thereby enhancing the overall linearity of the amplifier. The inductive degeneration also helps in extending the bandwidth by partially compensating for the capacitances present at the transistor's emitter and base, further improving the amplifier's high-frequency performance

3.5.Filter bank design in Q band

The procedure for designing the filter bank closely mirrored the approach used in the K band. However, meeting the performance specifications proved to be highly challenging. A significant issue was the reduction of the Q factors of the components at higher frequencies, leading to increased insertion loss and broader bandwidths. The latter effect was particularly problematic because the bandwidth greatly influences the amount of loss in the passband, as illustrated in Figure 36. This figure compares three fourth-order Chebyshev bandpass prototypes (with a return loss of 20 dB), all utilizing resonators with identical unloaded Q factors but differing bandwidths.

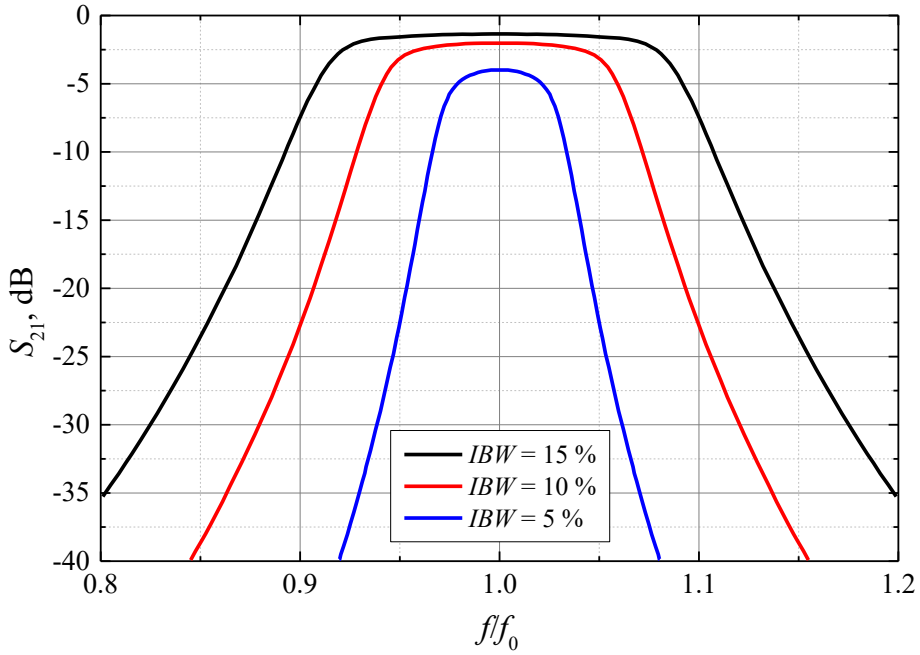


Figure 36. Illustration of compromise between instantaneous bandwidth and insertion loss

A filter with a narrower bandwidth experiences more passband loss since the resonator losses are concentrated within a smaller frequency range. This presents a trade-off: while a broader bandwidth reduces the filter's cut-off rate, it also minimizes passband loss. The optimal solution, therefore, is to maximize the bandwidth as much as possible without compromising the required cut-off rate and out-of-band rejection.

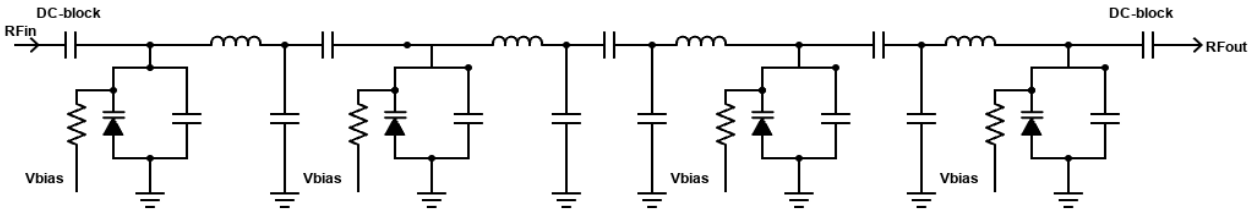


Figure 37. Final architecture of Q-band filter bank

After extensive optimization, the final schematic was achieved is illustrated in Figure 37. In short, the same 4th order tubular filter bank topology was used as in the K-band filter bank.

3.6. Amplifier design in Q band

In the Q band, a single-stage amplifier did not provide sufficient gain to compensate for the high insertion loss of the filter bank. Consequently, a two-stage amplifier had to be constructed. The design process for the two-stage amplifier followed a similar procedure to that of the single-stage amplifier in

terms of input and output matching. However, an additional step was required: conjugate interstage matching. This interstage matching was accomplished using the same *LC* matching pair technique to ensure optimal performance. By implementing this two-stage design, the amplifier was able to achieve the necessary gain to offset the significant insertion losses, thereby meeting the design specifications for the Q band filter bank. The schematic diagram of two stage Q band amplifier is provided in Figure 38.

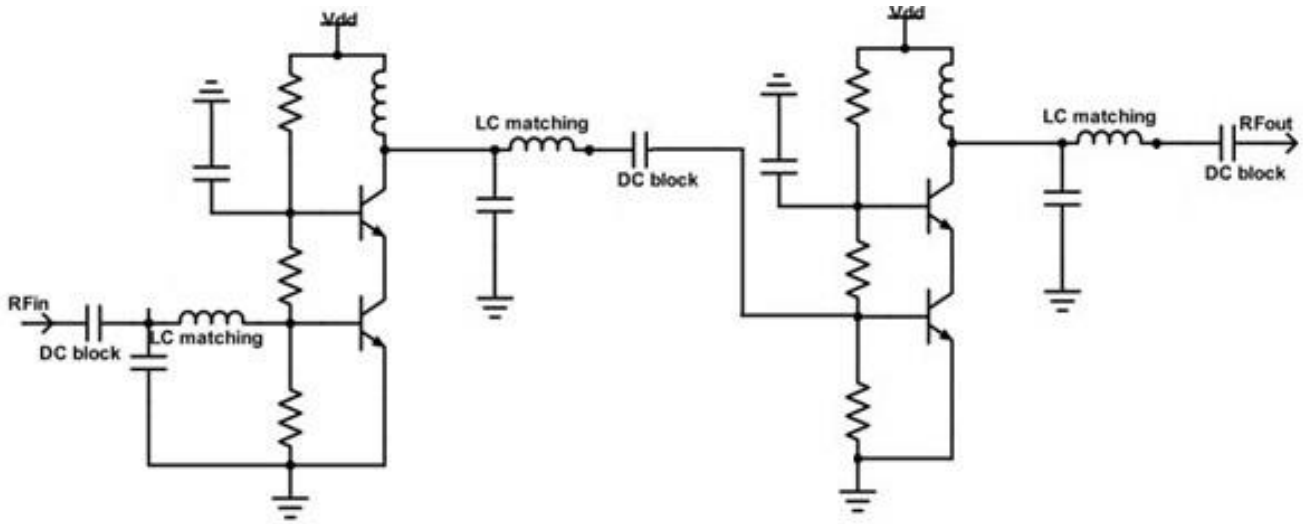


Figure 38. A two stage Q band cascode amplifier

4. Results

During this project, the MTBF was modeled and designed in the "Cadence Virtuoso ADE" environment. Each filter bank was treated as a two-port network, with its input and output terminated with 50 Ω loads. The following sections will present the simulation results at the schematic level, where parasitic component parameters are included, but mutual component coupling is not accounted for. After achieving satisfactory results in schematic level, the layout was prepared and the final electromagnetic computer modeling was carried out, evaluating all the parasitic parameters that affect the operation of the principal electrical circuit. To accomplish this, the EMX (Electromagnetic Extraction) software package was used, which accounts for all parasitic effects present in the topology, the electromagnetic interactions of interconnection lines, and so on. The results obtained from the computer modeling are presented in the next section.

4.1. Filter bank schematic results in K band

As mentioned previously, the filter banks in the K band were realized using a 4^{th} order tubular architecture. The entire K band was covered with two filter banks, as it was found that covering the entire band with just one filter bank would not yield acceptable results and, while using three filter banks would achieve better results, the complexity was not worth it, as the additional losses from the splitter and combiner would almost negate the gains.

First, looking at the S_{21} plot (Figure 39), it can be seen that excellent amplitude variability over the entire K band was achieved (< 1 dB). The worst-case insertion loss was 22.9 dB. The *IBW* varied between 1.34 and 1.7 GHz, which is well below the targeted bandwidth of 2 GHz, indicating a good outcome. The input and output return losses, indicated by S_{11} plots, were identical due to the symmetrical nature of the filter bank, with the worst-case return loss being 7.5 dB and the best-case return loss being 10.3 dB.

The biggest challenge in the K band was achieving satisfactory out-of-band isolation. To achieve a steeper roll-off, the order of the filter bank had to be increased from third to fourth, which resulted in more insertion loss. It can be seen from the S_{21} shape that the filter bank topology naturally provides better high-band isolation and worse low-band isolation. The best case of high-side out-of-band isolation was 48 dB, and the worst high-side case was 45 dB. The best case of low-side out-of-band rejection was 40.1 dB, and the worst case was 30.5 dB.

Comparing the results achieved at this stage with the targeted requirements, some insights can be made. The insertion loss is expected to be compensated by a single-stage amplifier, which typically shows about 20 dB gain at these frequencies. The return loss does not meet the requirements yet, but the output return loss largely depends on the amplifier's output matching, and the input return loss is expected to increase by at least 3 dB after implementing the input splitter. Overall, the parameters were deemed acceptable at this stage, so the process proceeded to the layout phase.

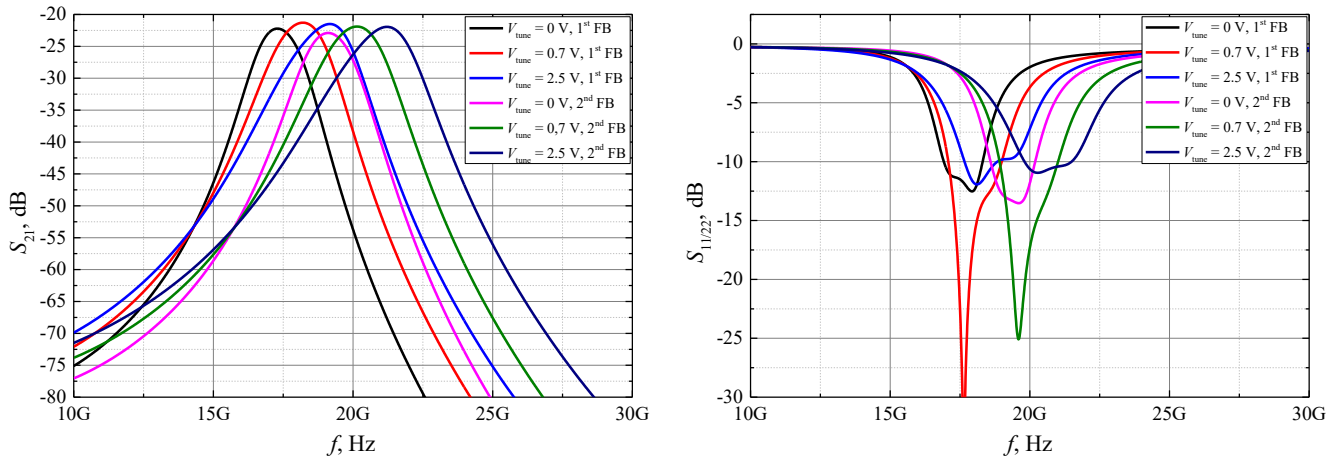


Figure 39. *S*-parameter simulation results of two filter banks (FB) in K band

4.2. Amplifier schematic results in K band

As discussed in the previous section on amplifier schematic design, the chosen topology was a single-stage cascode configuration. The aim was to achieve enough amplification for each filter bank to compensate for its insertion loss. In the K band, this meant that about 20 dB of amplification was needed. Additionally, requirements were set for return loss, with the output return loss being more critical as it would be seen at the output of the MTBF. The amplifier also provides reverse isolation when turned off. Another important aspect to consider was stability, with a target considerably more than 1, approximately 2.5. The *S*-parameter simulation results can be seen in Figure 40.

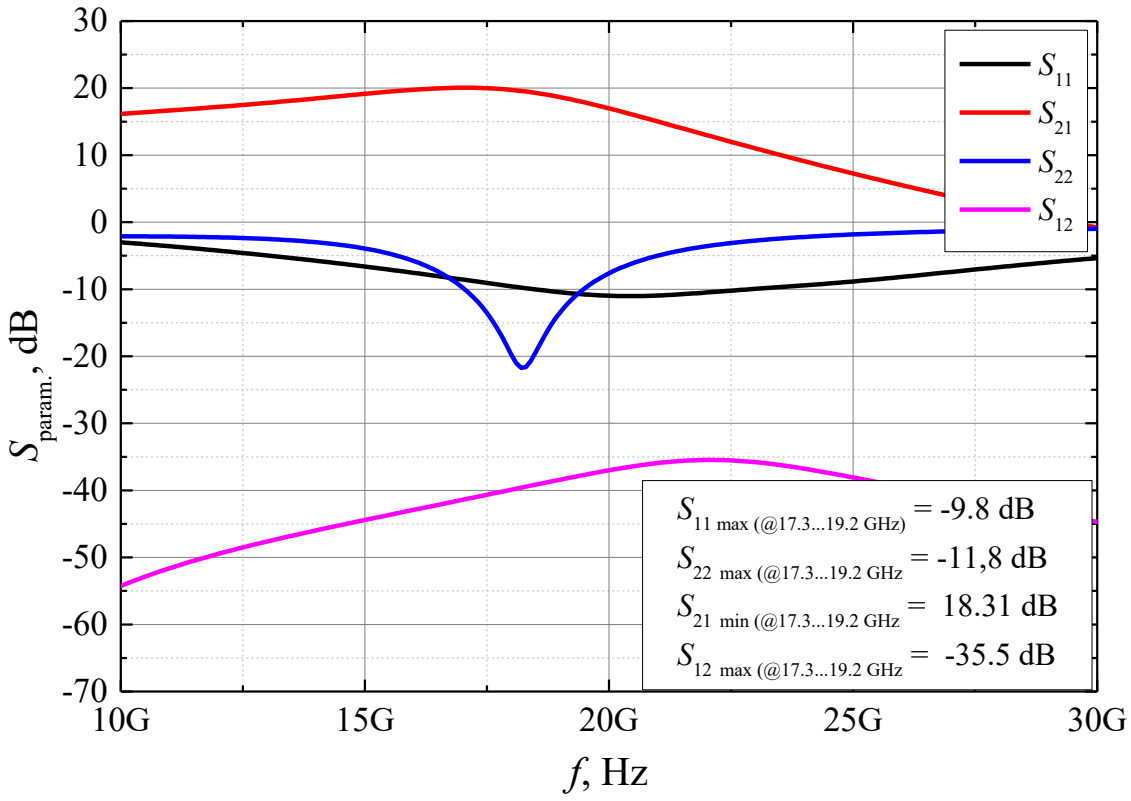


Figure 40. K band amplifier schematic results

Figure 40 displays the *S*-parameter simulation results for the lower frequency K band amplifier, optimized to work best in the frequency range of 17 – 19 GHz. From Figure 40, it can be seen that the minimum amplification value achieved in that range was 18.3 dB, with a maximum value exceeding 20 dB. Moreover, the input matching to 50 Ω was better than –9.8 dB, and the output matching, which was prioritized in this case, was better than –11.8 dB.

Figure 41 shows the K-factor dependency on frequency. The main takeaway here is that the minimum K-factor value was greater than 2.5, which was deemed sufficient to ensure stability during the MTBF manufacturing stage.

Finally, the harmonic balance results can be seen in Figure 42. This figure depicts the first and third harmonic output power dependency on input power, from which the OP_{1dB} and I*IP3* points are calculated. These were 4.2 dBm for OP_{1dB} and 12 dBm for *IIP3*, both of which were above the requirements set at this stage of the MTBF design process.

Overall, these results indicate that the amplifier design is on track to meet the necessary performance criteria, with sufficient amplification, good input and output matching, stability, and harmonic performance exceeding the required thresholds.

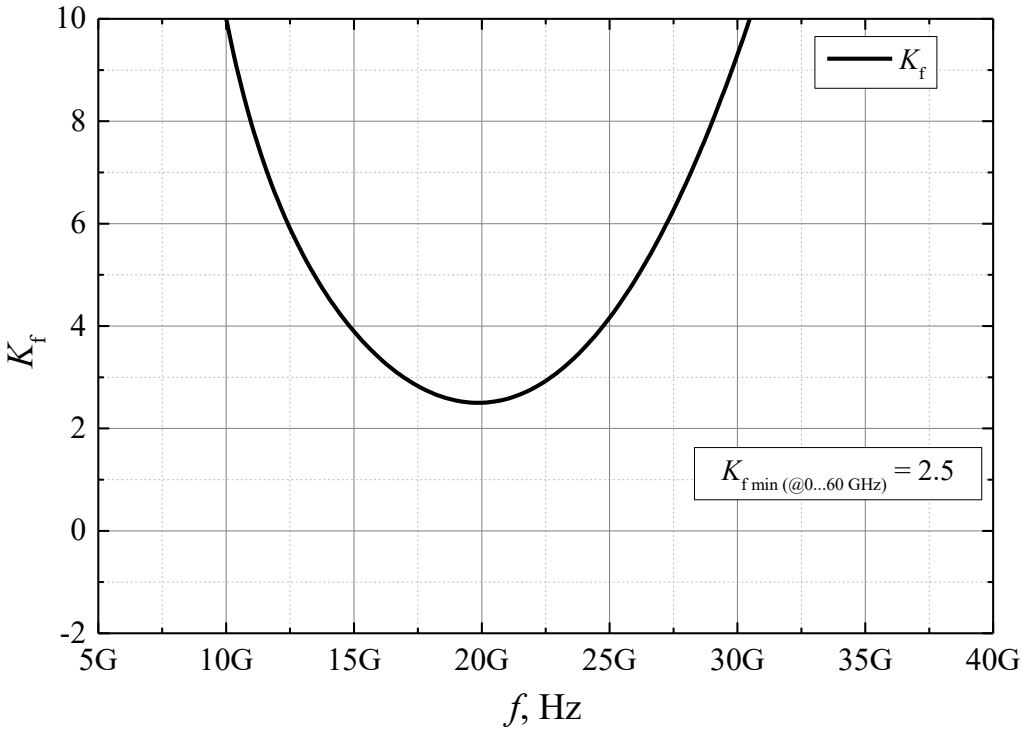


Figure 41. Stability factor dependency on frequency of K band amplifier

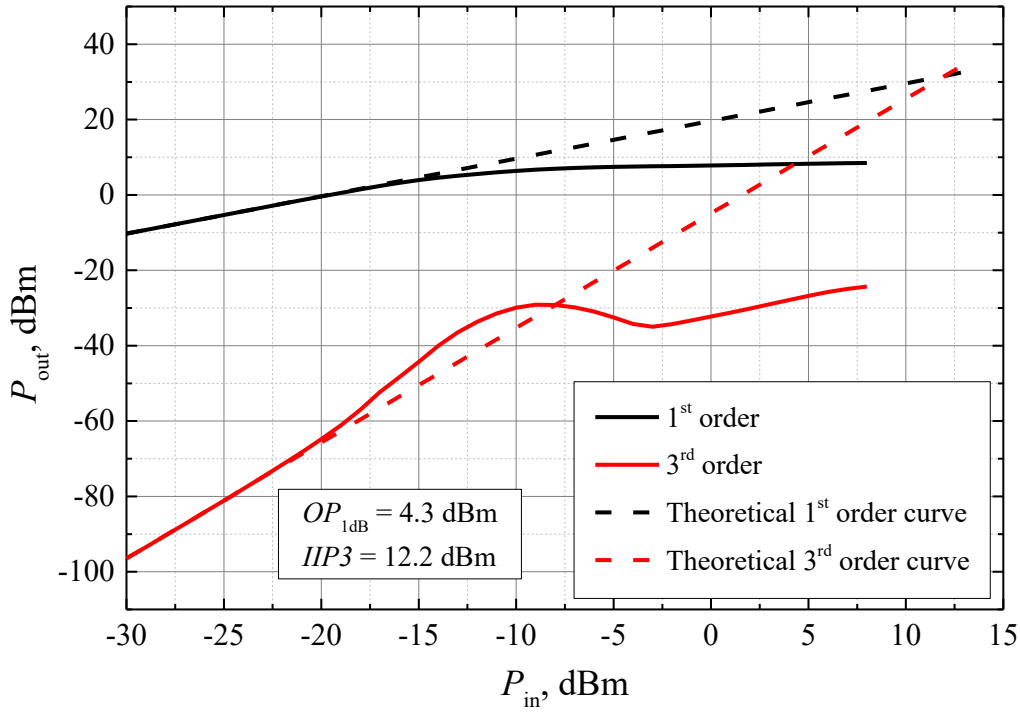


Figure 42. First and third order harmonic output power dependency on input power

4.3.Filter bank schematic results in Q band

The results of the Q band filter bank schematic simulation can be seen in Figure 43. It can be observed that, due to significantly lower component quality values at these frequencies, the insertion loss is substantially increased compared to the K band results. One of the main contributors to this was the attempt to achieve a narrow enough instantaneous bandwidth, which, as discussed earlier, can significantly contribute to insertion loss, especially given that the required *IBW* for the Q band is relatively smaller when compared to the center frequency.

Another thing to note is that the peak amplitude variation over the band is greater (< 4 dB) than in the K band. This is because varying the varactor voltage changes their quality by a greater amount in the Q band. In general, the parameters achieved were as follows: the worst-case insertion loss was 37 dB, the worst-case lower side out-of-band rejection was 40 dBc, and the worst-case high side rejection was 50 dBc. The return loss was no worse than 7.3 dB.

Overall, while the Q band filter bank exhibits higher insertion losses and greater amplitude variation, the achieved parameters were considered to be within acceptable limits for this design stage.

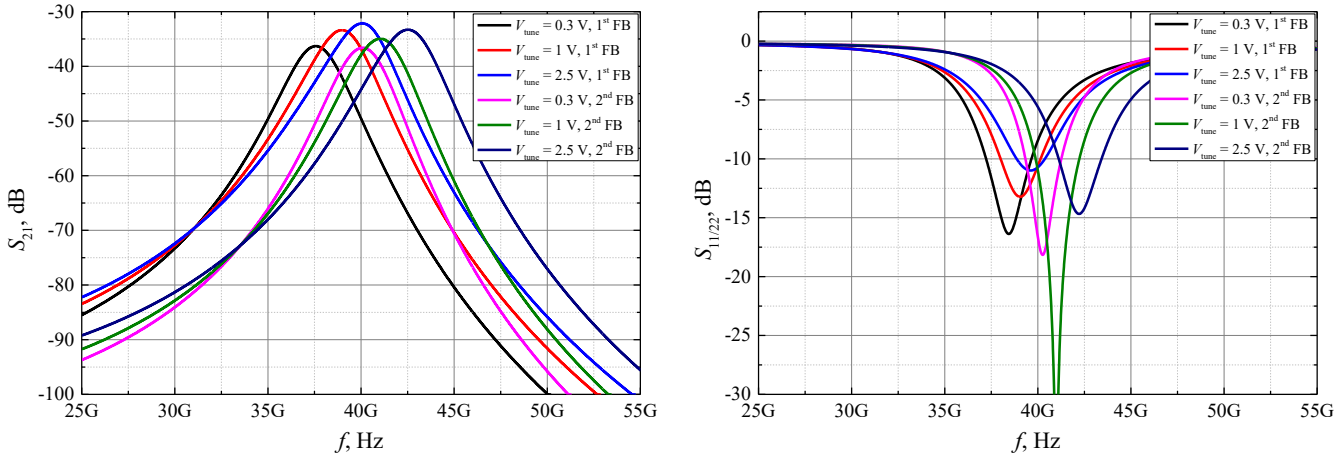


Figure 43. Q band filter banks schematic simulation results

4.4.Amplifier schematic results in Q band

As discussed in the previous section, the Q-band filter banks have significant insertion losses. Additionally, the intrinsic transistor gain decreases with increasing frequency. These factors necessitated the design of a two-stage amplifier for the Q-band. The main results from the *S*-parameter simulation are provided in Figure 44. The achieved amplification value in the Q-band was between 31 and 33 dB. This implies that combining such an amplifier with the designed filter bank would bring the insertion loss up to around 5 dB, making the amplification level sufficient. Moreover, it can be observed that the reverse

isolation doubles as two cascode stages are introduced, bringing it down to -66 dB. This ensures that the requirement for turned-off filter bank isolation is met. The input and output return loss of the amplifier showed great results, as both values were around -10 dB over the entire Q-band.

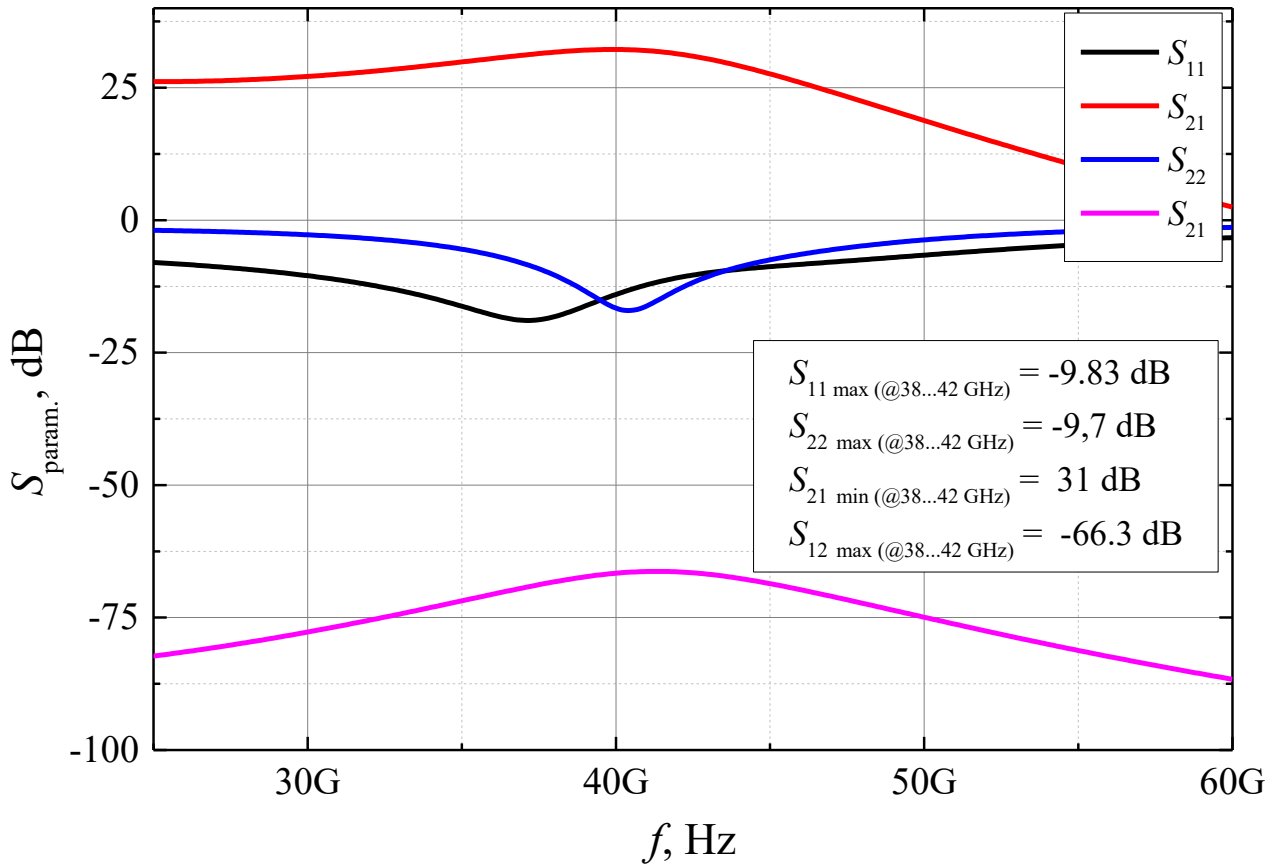


Figure 44. The *S*-parameter simulation results of a two stage Q band amplifier.

4.5. Filter bank post layout simulation results in K band

The filter bank schematic design proceeded to the layout design stage. Due to a non-disclosure agreement signed with the technology provider, no 3D layout views can be shown. Therefore, the layout procedure will largely be skipped, and only the final layout simulation results will be discussed.

In Figure 45, a comparison of the *S*-parameter results for one K band filter bank is presented. Results from only one filter bank are shown for clarity, as the results from the other lower frequency K filter bank were very similar.

The observations from this comparison are as follows: the overall S_{21} and S_{11} response within the 3 dB bandwidth was preserved during the layout stage, as shown in Figure 45. However, the out-of-band behavior changed quite significantly. On the low side, the overall rejection level increased slightly

compared to the schematic design, while on the high side, it was observed that the out-of-band rejection level saturated at above 80 dB, whereas the schematic results showed a continuous roll-off. These effects are most likely attributed to parasitic inductor coupling, which creates a parasitic path for the signal from the input port to reach the output port, thereby experiencing lower attenuation. This effect reduced the low side out-of-band isolation by 2 dB, making it 28 dBc at the worst corner, and actually improved high side rejection slightly, as the curve showed a slight undershoot before reaching the saturated level. Overall, the insertion loss decreased by 1.5 dB, likely due to parasitic effects from additional connections needed to join components, which inevitably introduce losses. The instantaneous bandwidth stayed below 2 GHz in post layout simulation as in was significantly smaller than 2 GHz in schematic design.

Summarizing the performance from post-layout simulation, it was concluded that the requirements still remained within the desired specifications.

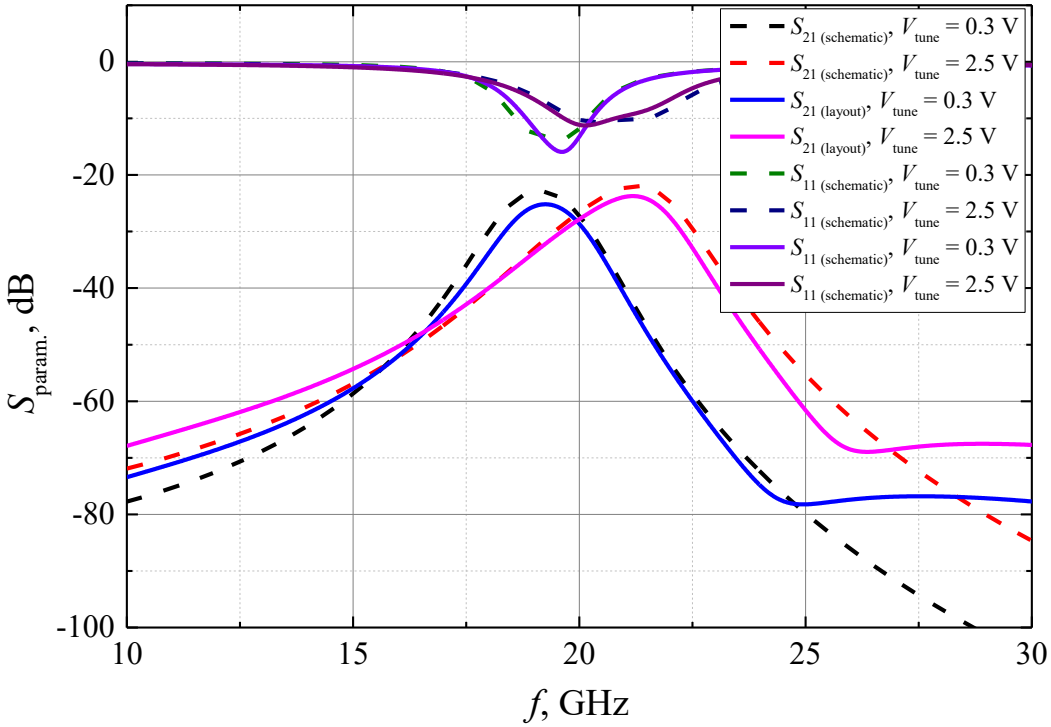


Figure 45. Schematic vs post layout simulation results of K band filter bank, covering frequencies 19 – 21 GHz

4.6.Filter bank post layout simulation results in Q band

The aforementioned effects were much more pronounced in the Q band. The initial design, which closely followed the K band design, showed significant performance degradation when the entire filter bank was laid out and simulated (Figure 46). These issues only became apparent when smaller blocks

were combined into a single layout. It was concluded that the likely culprit was parasitic inductor coupling. To test this hypothesis, a cross-pattern shield, example of which is given in Figure 47, was added underneath the outer inductors. This proved to be a successful approach, as the results from the layout simulation with inductor shielding closely resembled those obtained from schematic simulations.

The comparison between the post-layout simulation and the schematic filter bank simulation is provided in Figure 46. It can be seen that after adding inductor shielding, the outcome was in line with the one observed in the K band. The low-side rejection tended to decrease by 2-3 dB, and the high-side out-of-band rejection either did not change or improved slightly due to the same undershoot observed in the S21 curve. The overall out-of-band rejection remained above 38 dB.

Again, the in-band performance did not change significantly. The insertion loss increased by 1 dB, and the instantaneous bandwidth (*IBW*) remained the same as in the schematic design, with a worst-case value of 2.05 GHz. These adjustments ensured that the design met the desired specifications, demonstrating that inductor shielding is a crucial element in maintaining performance integrity at higher frequencies.

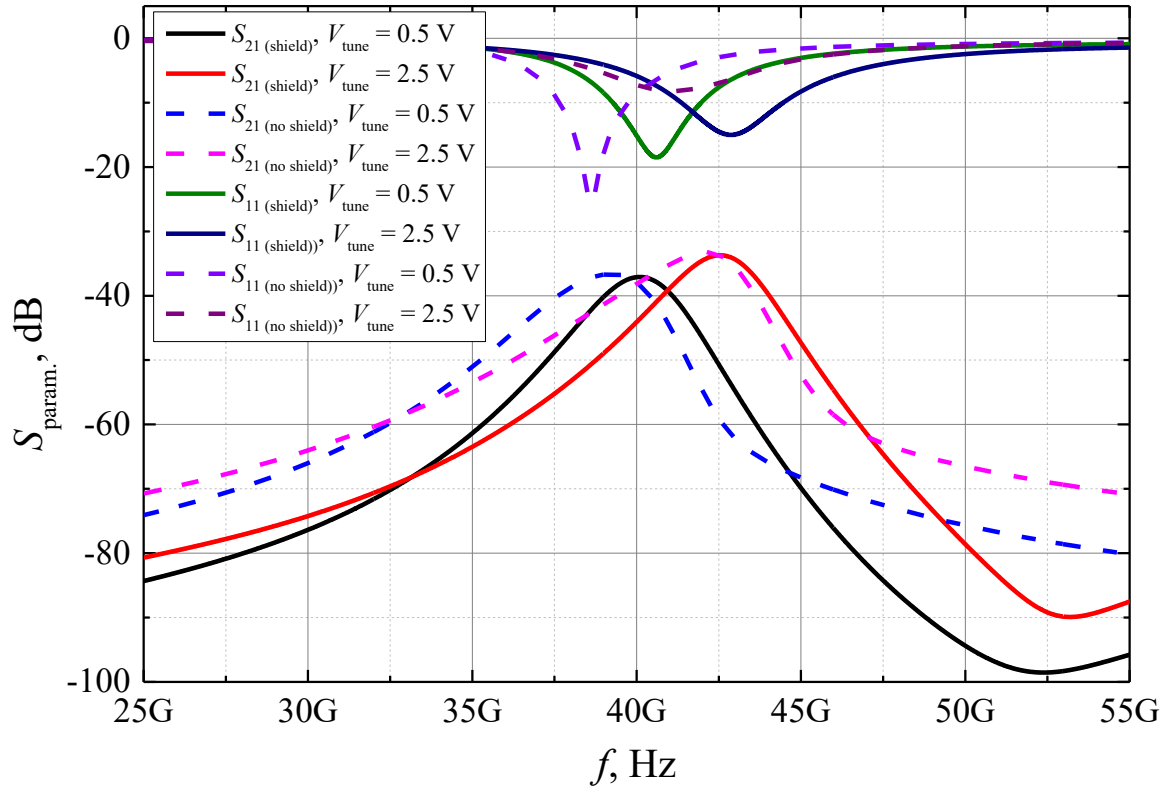


Figure 46. Comparison of *S*-parameters between designs with inductor shielding and no inductor shielding

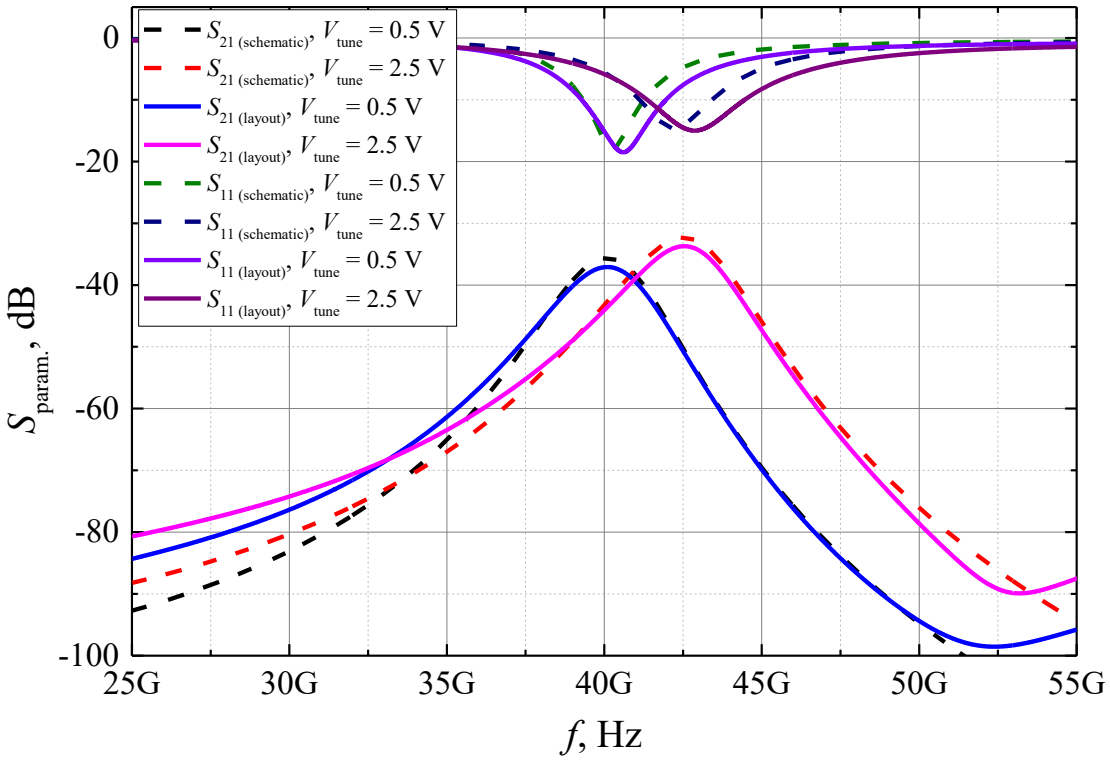


Figure 47. Schematic vs post layout simulation results of Q band filter bank

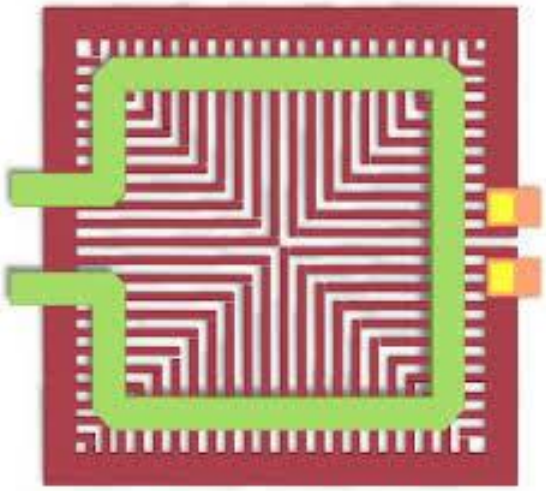


Figure 48. Inductor shielded with cross ground pattern [30].

Finally, the last result that needs to be discussed is the group delay simulation. Figure 49 shows the AC simulation results for both K and Q filter banks. The main conclusion from these results is that the group delay values in both cases stay significantly below the requirements set for the project.

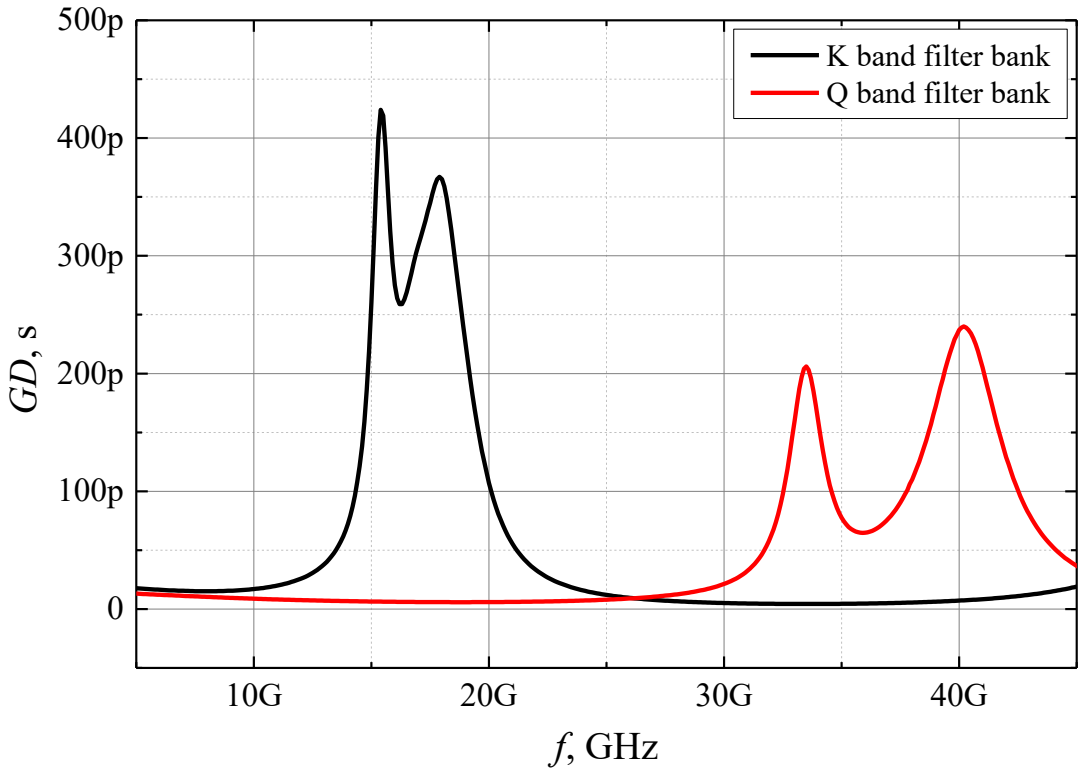


Figure 49. Group delay response for K and Q band filter banks.

Additionally, it is important to note that the group delay increases for lower frequency filters. This phenomenon occurs because, at lower frequencies, the reactive components (inductors and capacitors) in the filter have a more pronounced effect on the phase response of the signal. Specifically, lower frequency filters typically have larger inductance and capacitance values to achieve the desired filtering characteristics, leading to a slower response time. Consequently, the signal takes longer to pass through the filter, resulting in a higher group delay.

4.7. Discussion

Both the K and Q bands were covered with two filter banks each. The S_{21} response in the K band demonstrated excellent amplitude variability over the entire K band (< 1 dB). The worst-case insertion loss in the post-layout simulation was 25.5 dB, and the *IBW* ranged between 1.34 and 1.7 GHz, well below the targeted bandwidth of 2 GHz. This indicates a successful outcome. The biggest challenge in the K band remains achieving satisfactory out-of-band isolation, although with minor tuning, it should be brought up from the current 28 dB to the specification value of 30 dB.

The Q band design proved challenging from another perspective. The key challenge in this band is maintaining a narrow enough instantaneous bandwidth. However, even in post-layout simulations, the worst-case *IBW* value was 2.05 GHz, which was very close to the targeted performance. This indicates that the design is on track to meet the necessary performance criteria for the Q band, despite the difficulties. The successfully achieved results show that the selected topology and design procedure are suitable for the realization of the MTBF.

Given that the performance achieved is close to the targeted values, the final MTBF is expected to be competitive with state-of-the-art solutions discussed previously in this thesis. The comparison is made again and provided in Table 2. Looking at the table, it can be seen that the proposed MTBF is most competitive in design compactness. The especially narrow instantaneous bandwidth in the Q band also stands out. Additionally, it should be noted that the proposed filter covers two frequency bands simultaneously, which is a solution not yet implemented in state-of-the-art designs. This makes it not only competitive in performance but also the only solution covering both emerging frequency spectra for LEO satellites while occupying a small on-chip area. Utilizing well-established technology, this design is highly integrable, making it a significant advancement in the field.

Table 2. A comparison of proposed MTBF with state of the art found in scientific literature

Technology	*BW*, GHz	*IL*, dB	*IBW*, GHz	*Isolation*, dBc	P_{DC}, mW	Chip area, mm²
This work, 55 nm BiCMOS	17 – 21, 37.5 – 42.5	5	< 2.05	< -28 in K band, < -38 in Q band	50	< 1
[19] MEMS	21.69 –24.36	4	< 0.9	< -20	N/A	2.25
[20] GaAs P-HEMT	9 – 15	10 Gain	< 2	< -40	N/A	6
[21] 150 nm P-HEMT	17.5 – 21.5	10	0.9	< -40	50	1
[23] 130 nm SiGe	42.5 – 51.0	8.4	4	38 - 58	31.5	4.7

Conclusions

1. The post-layout simulation results in the K band show that the proposed MTBF can achieve an insertion loss better than 10 dB, out-of-band isolation better than 28 dBc, instantaneous bandwidth smaller than 1.8 GHz, input return loss better than 8 dB, and output return loss better than 12 dB, making it competitive with state-of-the-art solutions.
2. The results of post-layout simulations in the Q band indicate that the suggested MTBF design is capable of achieving an insertion loss surpassing 10 dB, out-of-band isolation exceeding 38 dBc, instantaneous bandwidth below 2.1 GHz, input return loss superior to 8 dB, and output return loss better than 12 dB, positioning it as a competitive contender among state-of-the-art solutions.
3. Schematic and post-layout simulations show the biggest difference in out-of-band performance, while in-band parameters stay consistent, indicating that early design should focus on improving out-of-band isolation, with careful layout decisions later to optimize this performance parameter.

References

[1] Pantoli, L.; Leuzzi, G.; Deborgies, F.; Jankovic, P.; Vitulli, F. A Survey of MMIC Active Filters. Electronics 2021, 10, 1680. https://doi.org/10.3390/electronics10141680

[2] D. Tiradossi, A. Cazzorla, L. Pelliccia, M. Bartocci, P. Bia and A. Manna, "Planar and Low-consumption Switchable Filter Banks with Tunable Passband and Stopband Responses," 2021 IEEE MTT-S International Microwave Filter Workshop (IMFW), Perugia, Italy, 2021, pp. 224-226, doi: 10.1109/IMFW49589.2021.9642281.

[3] Razavi, B., RF Microelectronics (Prentice Hall Communications Engineering and Emerging Technologies) 2nd Edition.

[4] Kurokawa, K., "Power Waves and the Scattering Matrix," IEEE Trans. Microwave Theory Tech., Vol. 13, No. 2, March 1965, pp. 194–202

[5] MARSH, S. Practical MMIC Design. Artech House, 2012. ISBN-10: 1-59693-036-5

[6] D.E. Johnson. Introduction to filter theory. Prentice-Hall electrical engineering series. Prentice-Hall, 1976. 3, 8, 49

[7] D.M. Pozar. Microwave engineering. J. Wiley, 2005.

[8] G.L. Matthaei, L. Young, and E.M.T. Jones. Microwave filters, impedance-matching networks, and coupling structures. Artech House microwave library. Artech House Books, 1980.

[9] I.C. Hunter and Institution of Electrical Engineers. Theory and design of microwave filters. IEE electro-magnetic waves series. Institution of Electrical Engineers, 2001.

[10] Ikuo Awai. Meaning of resonator's coupling coefficient in bandpass filter design. Electronics and Communications in Japan (Part II: Electronics), 89(6):1–7, 2006.

[11] J.B. Ness. A unified approach to the design, measurement, and tuning of coupled-resonator filters. Microwave Theory and Techniques, IEEE Transactions on, 46(4):343 –351, apr 1998.

[12] B.S. Guru and H.R. Hızıroglu. Electromagnetic field theory fundamentals. Cambridge University Press, 2004.

[13] P.W. van der Walt. Microwave networks lecture notes. June 2010

[14] D.A. Neamen. Microelectronics: circuit analysis and design. McGraw-Hill, 2007.

[15] Skyworks Solutions, Inc. Application Note: Varactor Diodes, Rev. A edition, August 2008.

[16] G.D. Vendelin, A.M. Pavio, and U.L. Rohde. Microwave circuit design using linear and nonlinear techniques. Wiley, 2005

[17] I.C. Hunter and J.D. Rhodes. Electronically tunable microwave bandpass filters. Microwave Theory and Techniques, IEEE Transactions on, 30(9):1354 –1360, sep. 1982.

[18] A.R. Brown and G.M. Rebeiz. A varactor-tuned RF filter. Microwave Theory and Techniques, IEEE Transactions on, 48(7):1157 –1160, jul 2000.

[19] Deng, Z.; Wei, H.; Guo, X. 21.69–24.36 GHz MEMS Tunable Band-Pass Filter. Micromachines 2016, 7, 149. https://doi.org/10.3390/mi7090149

[20] F. Bergeras, P. Duême, J. -P. Plaze, L. Darcel, B. Jarry and M. Campovecchio, "Novel MMIC architectures for tunable microwave wideband active filters," 2010 IEEE MTT-S International Microwave Symposium, Anaheim, CA, USA, 2010, pp. 1356-1359, doi: 10.1109/MWSYM.2010.5517593.

[21] Fan, K.; Weng, C.; Tsai, Z.; Wang, H.; Jeng, S. K-band MMIC active band-pass filters. In IEEE Microwave and Wireless Components Letters; IEEE: Piscatway, NJ, USA, 2005; Volume 15, pp. 19–21.

[22] Pantoli, L.; Leuzzi, G.; Deborgies, F.; Jankovic, P.; Vitulli, F. A Survey of MMIC Active Filters. Electronics 2021, 10, 1680. https://doi.org/10.3390/electronics10141680

[23] A. Moradinia, C. D. Cheon, C. T. Coen, N. E. Lourenco, A. S. Cardoso and J. D. Cressler, "A 42.5–51.0 GHz SiGe BiCMOS Integrated Tunable Bandpass Filter and Attenuator," 2022 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS), Phoenix, AZ, USA, 2022, pp. 183-186, doi: 10.1109/BCICTS53451.2022.10051694

[24] https://www.ksat.no/globalassets/ksat/documents/ksat_white_paper.pdf

[25] P. Chevalier et al. A 55 nm triple gate oxide 9 metal layers SiGe BiCMOS technology featuring 320 GHz fT / 370 GHz fMAX HBT and high-Q millimeter-wave passives. Feb., 2015.

[26] https://markimicrowave.com/technical-resources/tools/lc-filter-design-tool/

[27] B. Landgraf, "MOM Capacitance Measurements in a 130 nm CMOS Node," 2015 Austrian Workshop on Microelectronics, Vienna, Austria, 2015, pp. 42-45, doi: 10.1109/Austrochip.2015.10.

[28] Jinglin Shi, A. Sidelnicov, Kok Wai J. Chew1, Mei See Chin1, C. Schippel, J.M.M. dos Santos, F. Schlaphof, L. Meinshausen, John R. Long, D.L. Harame. Evolution and Optimization of BEOL MOM Capacitors Across Advanced CMOS Nodes

[29] Po-Yen Chiu and Ming-Dou Ker, “Metal-layer capacitors in the 65 nm CMOS process and the application for low-leakage power-rail ESD clamp circuit,” in Microelectronics Reliability 54 (2014) , pp.64–70.

[30] P. Agarwal et al., "Switched Substrate-Shield-Based Low-Loss CMOS Inductors for Wide Tuning Range VCOs," in IEEE Transactions on Microwave Theory and Techniques, vol. 65, no. 8, pp. 2964-2976, Aug. 2017, doi: 10.1109/TMTT.2017.2675423.