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Fabrication of III-V semiconductor monolithic integrated mid-infrared photonic system

Master‘s final thesis

Photonics and nanotechnology study programme

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Introduction

Semiconductor lasers are fundamental components of modern optoelectronic systems, recognized for their compact size, efficiency, and versatility. Within this category, quantum cascade lasers (QCLs) represent a distinguished class of devices operating on intersubband electron transitions within engineered quantum well structures. This mechanism enables emission in the mid- to long-infrared spectral range (3–25 μm), which is particularly important due to the presence of atmospheric transparency windows and the unique absorption "fingerprints" of many molecules. As a result, mid-infrared radiation is highly suitable for applications such as environmental monitoring, industrial safety, and medical diagnostics, where precise detection of gases like carbon dioxide (CO_2) and methane (CH_4) is essential [1]. These gases are among the primary contributors to greenhouse effects, making their accurate detection crucial for climate research and pollution control [2].

The InAs/AlAsSb material system is especially promising for mid-infrared QCL applications due to its favorable electronic and structural properties. A large conduction band offset of around 2.1 eV enables the precise engineering of electron transitions, ensuring efficient emission of light at wavelengths that are relevant for gas sensing [3]. Additionally, the low effective electron mass in InAs contributes to reduced threshold current and enhanced optical gain, improving device performance, particularly at elevated temperatures typical for portable sensing systems [4].

At the same time, advances in laser technology have led to quick improvements in photonic integrated circuit (PIC) systems. The integration of multiple optical components including lasers, photodetectors, and waveguides onto a single chip has become increasingly important for realizing compact, stable, and energy-efficient systems [5]. However, achieving reliable monolithic integration of mid-infrared photonic devices remains a significant technological challenge, largely due to the complexity of fabrication processes, which represents the most demanding aspect of this work. The performance of integrated systems is highly dependent on the quality of micro- fabrication. Key components such as waveguides, resonators, and laser cavities require highly controlled geometries, including anisotropic etching profiles (deep dry etching), smooth and vertical sidewalls, and minimal surface roughness. However, deep dry etching processes require high ion energies to achieve anisotropy, and this can lead to ion-induced damage and redeposition of etching by-products. Additionally, any imperfections during the fabrication can introduce optical scattering losses, degrading waveguide performance and laser efficiency [6]. For laser cavities, well-defined and smooth mirror facets are essential to ensure effective optical feedback and stable lasing modes.

Thus, **the aim of this work** is to fabricate monolithically integrated mid-infrared quantum cascade lasers and quantum cascade detectors photonic system.

Tasks for this work:

1. Development of the microfabrication process.
2. Formation of a hard mask for III-V device fabrication.
3. Characterization of the optical and electrical properties of fabricated devices.

1. Literature review

1.1. Quantum cascade detectors

Quantum cascade detectors (QCDs) are unipolar photodetectors based on intersubband transitions in quantum-engineered semiconductor heterostructures, enabling the detection of photons with energies below the material bandgap and thus operation in the mid-infrared to terahertz range [7]. In QCD electrons undergo transitions between quantized states within the conduction band while remaining free in the in-plane direction. The schematic representation of QCD is shown in Fig. 1. Their band structure is formed by stacking thin layers of materials with different conduction band offsets resulting in a periodic sequence of quantum wells and barriers. Each period consists of an n-doped optically active well, where photon absorption promotes electrons to higher subbands, coupled to a cascade extractor that drives carrier transport through tunneling and longitudinal optical phonon-assisted scattering [7]. This engineered cascade creates an internal potential gradient, allowing directional electron flow and photocurrent generation even in photovoltaic (zero-bias) operation, which significantly reduces dark current and noise [8].

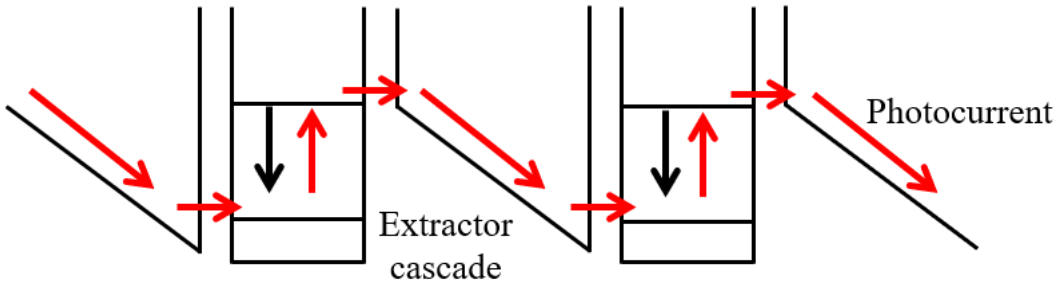

Fig. 1. Schematic conduction-band diagram of a QCD (adapted) [8].

To evaluate the performance of QCDs, a key parameter is the specific detectivity (D^*). Detectivity is derived from the noise equivalent power (NEP), which represents the optical power required to generate a photocurrent equal to the noise current. It is defined as the inverse of NEP, normalized by the detector area A and the measurement bandwidth Δf, as shown in formula 1 [7].

$$D^*(v) = \frac{\sqrt{A \cdot \Delta f}}{\mathrm{NEP}} = \frac{R(v) \cdot \sqrt{A \cdot \Delta f}}{i_\mathrm{n}} \ [\mathrm{Jones}] \qquad (1)$$

There R identifies as responsivity, the ratio between the photocurrent exiting the detector and the optical power generating it (formula 2) [9].

$$R = \frac{I}{P_\mathrm{opt}} \ [\frac{\mathrm{A}}{W}] \qquad (2)$$

In QCDs, the sample geometry plays a crucial role due to the polarization selection rule, which states that only the electric field component perpendicular to the quantum well layers (i.e., along the growth direction) can induce optical transitions. Consequently, the device must be designed so that light propagates inside the structure with a non-zero component along this direction. Fig. 2 shows three common QCD detector geometries.

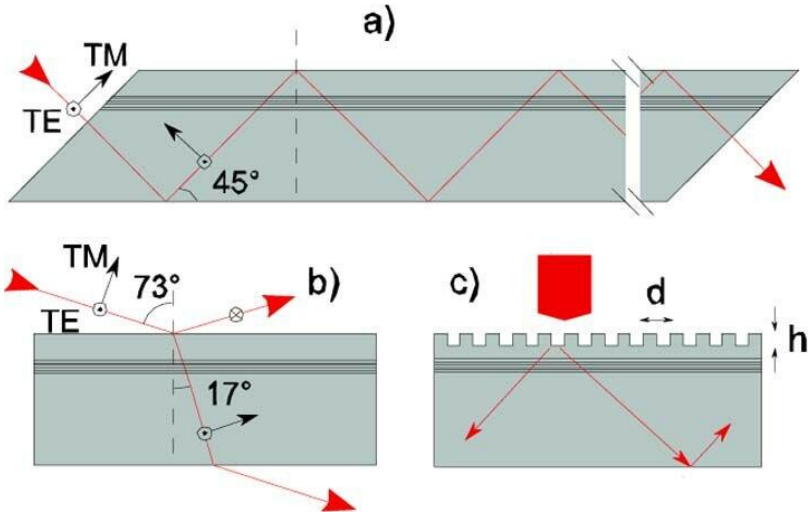

Fig. 2. Schemes of different QCD device geometries. a) 45° multipass waveguide, b) Brewster angle configuration and c) grating coupler [8].

In the 45° wedge configuration (Fig. 2a), the sample is polished at an angle so that the incident beam enters indirectly, undergoing multiple internal reflections that increase the optical path length and interaction with the active region. This geometry is relatively simple to fabricate and provides robust and reproducible characterization, which is why it is widely used for measuring the performance of QCD devices [8]. The main advantage of this configuration is its wavelength-independent sensitivity. In the Brewster geometry, the sample is illuminated at the Brewster angle (Fig. 2b). This is the specific incidence angle at which TM-polarized light experiences zero reflection at the interface, meaning that the incoming light is fully transmitted into the semiconductor [10]. Consequently, the electric field within the structure is maximized, thereby enabling efficient coupling to intersubband transitions. This approach requires minimal sample preparation compared to the 45° wedge geometry, making it experimentally convenient. However, it is important to note that the overall conversion efficiency of such devices is typically low since the light passes through the active region of the device only once, and there is no optical confinement [8]. A third approach uses diffraction gratings (Fig. 2c) to enable normal-incidence operation, where the periodic surface scatters light and generates an electric field component along the growth direction, satisfying the ISB selection rule without the need for oblique illumination [8]. This geometry is particularly attractive for practical applications, as it supports compact optical setups and straightforward integration into photonic systems.

1.2. Quantum cascade lasers

Semiconductor light sources can be classified into two main groups based on the photon emission mechanism: interband semiconductor light sources and intersubband light sources. In the first case, a photon is emitted during the recombination of an electron in the conduction band and a hole in the valence band (Fig. 3 left). In the second case, a photon is emitted in a quantum well within the conduction band during an electron's transition from a higher-energy subband to a lower-energy subband (Fig. 3 right).

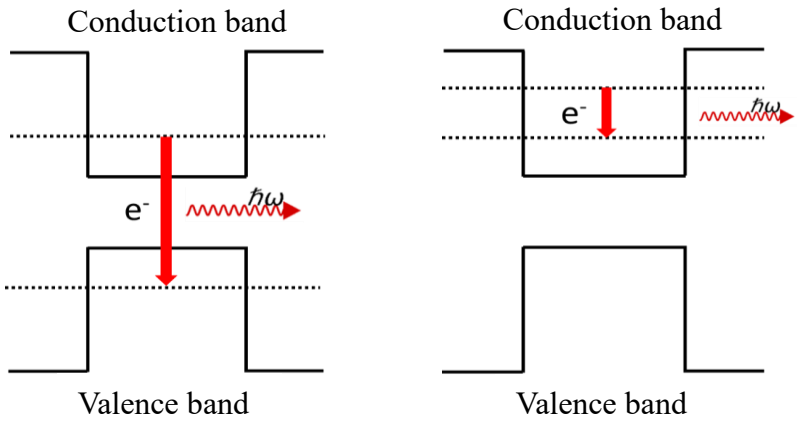

Fig. 3. Electron recombination with a hole emitting a photon (left) and electron transition in the conduction band to a lower subband emitting a photon (right).

Quantum cascade lasers (QCLs) are semiconductor lasers that generates radiation through intersubband electron transitions in quantum wells, which act as a light source [11]. QCL was first proposed and demonstrated by Jerome Faist, Federico Capasso, and their team at Bell Laboratories in 1994. Unlike conventional lasers, QCLs operate in the mid-infrared to terahertz range, making them highly valuable for applications such as spectroscopy, chemical sensing, and medical diagnostics [12]. Its structure consists of periodic sequences (cascades) of quantum wells and barriers, forming an active region where optical amplification occurs due to electron transitions between energy levels in the conduction band. The active region is surrounded by cladding and waveguide layer pairs with a lower refractive index, which confine the optical mode, ensuring efficient light propagation. The resonator, often designed as a Fabry-Perot cavity or a distributed feedback (DFB) structure, amplifies the generated radiation, ensuring coherent emission [12].

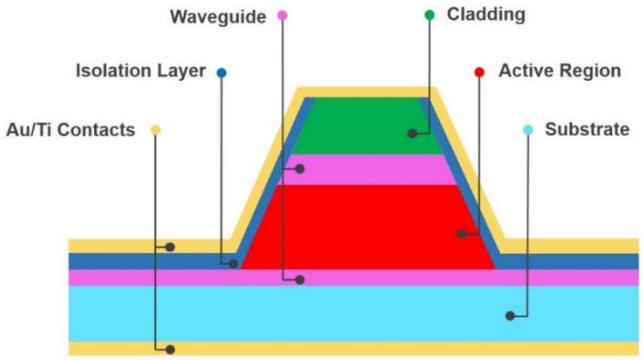

Fig. 4. Schematics representation of a QCL laser diode, where radiation is emitted from the active region [13].

Unlike traditional laser diodes, a QCL is a unipolar device that requires only one type of charge carrier - electrons. Their conduction band diagram shows that a flow of injected electrons passes through multiple periodically repeating active regions, emitting a photon in each. Due to this cascaded structure, a single injected electron can generate many - often 20–40 photons (depending on number of cascades), significantly increasing quantum efficiency.

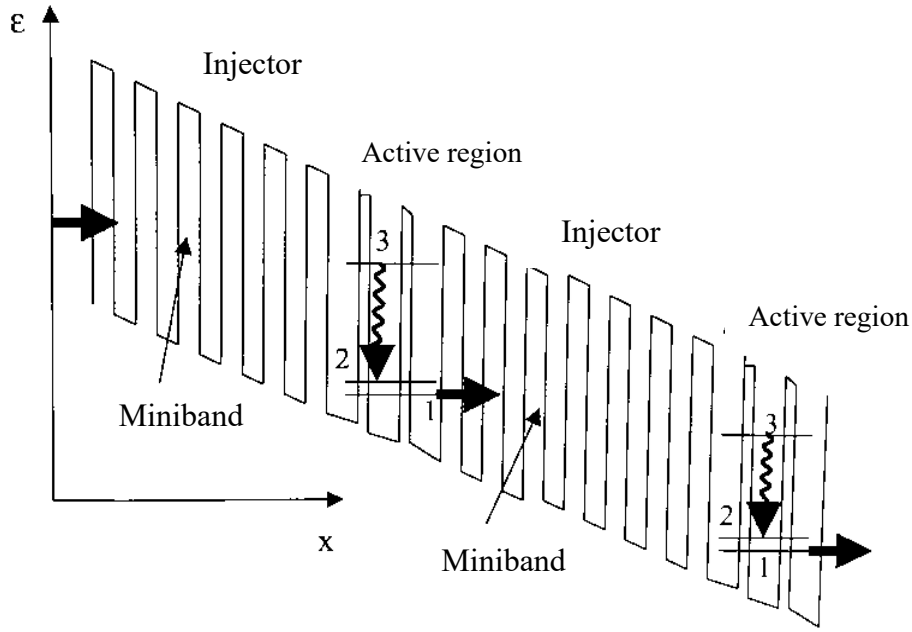

Fig. 5. Fragment of the conduction band structure of QCL with quantum wells in the active regions [14].

The active regions of QCLs can consist of quantum wells, as shown in Fig. 5, or superlattices. Quantum wells are separated by barriers made of wider bandgap materials, through which electrons can tunnel. The tunneling probability greatly increases when there is a state of the same energy level on the other side of the barrier (resonant tunneling). The regions between active areas, called injectors, are designed to transport a relaxed electron from a lower energy level in one active region to a higher energy level in the next. Injectors typically have thin barriers, forming superlattices where electrons move freely within minibands, and the narrow miniband width ensures that their energy distribution does not broaden.

Although practical QCL structures contain multiple quantized energy subbands within each cascade period, their operating principle is commonly described using a simplified three-level model consisting of an upper lasing state, a lower lasing state, and an injector/extraction state. Under an applied electric field of approximately 70 kV/cm, electrons are transported through the structure and injected via resonant tunneling from the injector miniband into the upper lasing state (level 3) of the active region. Since this level is not thermally excited, the laser can operate even at room temperature [14]. Stimulated photon emission occurs through an intersubband transition from level 3 to level 2. Subsequently, electrons rapidly relax from level 2 to level 1 through longitudinal optical (LO) phonon scattering and are injected into the next cascade stage via resonant tunneling, where the process repeats.

For efficient laser operation, the electron lifetime in the upper lasing state must be longer than in the lower lasing state to maintain population inversion. Therefore, the relaxation time from level 3 to level 2 ($\tau_{32} \approx 3$ ps) must exceed the electron lifetime in level 2 ($\tau_2 \approx 2.6$ ps). To ensure the lower lasing state is rapidly depopulated, the energy separation between levels 2 and 1 is designed to match the LO phonon energy. This enables efficient phonon-assisted scattering and prevents electron accumulation in the lower state.

The second highly significant advantage of this type of semiconductor laser is their unipolarity, which prevents their operation from being hindered by non-radiative Auger recombination, allowing them to operate at significantly higher temperatures compared to interband laser diodes [15]. For the same reason, these lasers can function at very low photon energies, i.e., at long emission wavelengths. Thus, quantum cascade lasers are the only type of semiconductor laser diode that covers the entire mid infrared and far-infrared radiation spectrum.

1.3. III-V semiconductors for QCL

The choice of material system for developing mid-infrared wavelength QCLs is primarily determined by the conduction band discontinuity (ΔE_c) of the well and barrier materials, as this enables higher subband energies and larger subband separation, consequently allowing for higher intersubband transition energies. By varying the width of the active quantum well, the spacing between these energy levels can be adjusted, allowing the creation of QCL for different wavelengths using the same material system [12]. Naturally, a shorter emission wavelength requires a larger conduction band offset. Fig. 6 shows the conduction band alignments of different material systems used in the development of QCL.

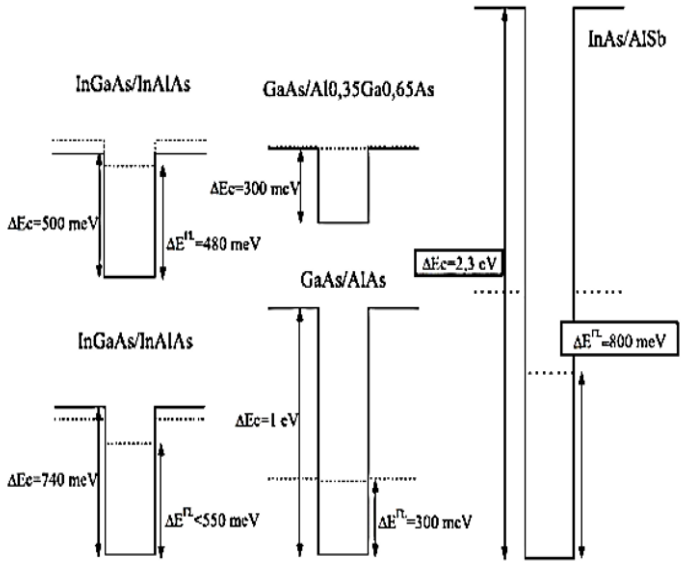

Fig. 6. Conduction band offset of different material systems used for development of QC lasers [16].

It can be observed that InAs/AlSb has the largest conduction band offset. However, there is another factor that determines the maximum possible energy of the emitted photon - the energy position of the side valley, depicted in the aforementioned figure as a dashed line. This limits the position of the highest excited electron level that can be used for electron transitions in the quantum well. It is evident that in the InAs/AlSb material system, this energy is also higher than in other material systems.

Another equally important parameter that characterizes laser performance is the electron effective mass in the quantum well [12]. The gain coefficient of the laser's active medium is inversely proportional to the electron effective mass, meaning a smaller electron effective mass results in higher gain in the laser's active medium. This value is also the most favorable in the InAs/AlSb material system. For these reasons, the InAs/AlSb material system was chosen for the development of QCL used in this work.

An equally significant parameter is the compatibility between the material system and the substrate material. The diagram (Fig. 7) shows the positions of the valence and conduction bands of different semiconductor compounds, as well as the crystal lattice constants, depending on the composition of the compounds. This diagram purposefully illustrates the principles by which materials and substrates for semiconductor emitters are selected, on which these structures can be grown. The diagram is applicable to both interband and intersubband semiconductor light sources.

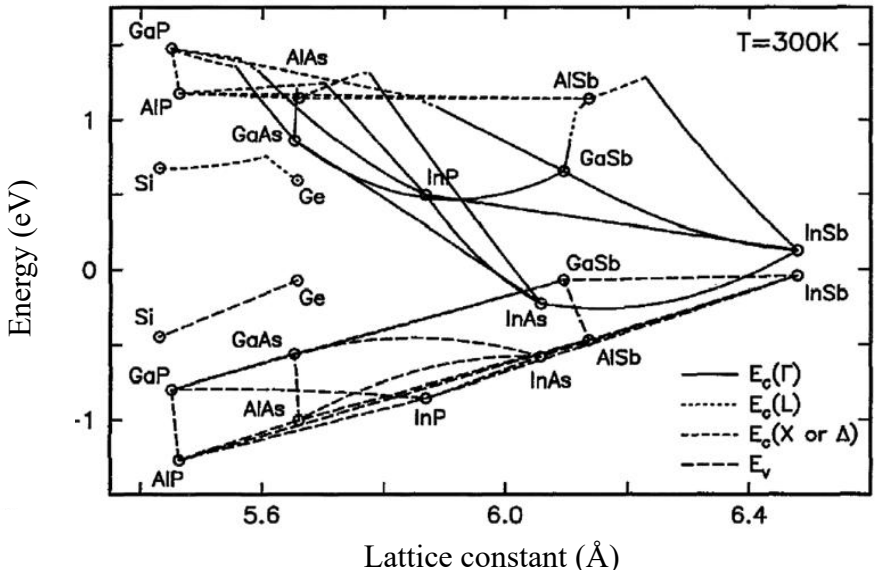

Fig. 7. Energy diagram of different semiconductor materials, indicating the position of the conduction band and the valence band, aligned with the Fermi level position at the top, depending on the material's crystal lattice constant [17].

1.4. Fabrication: principles of photolithography

Optical lithography/photolithography is used in the manufacturing of semiconductor devices. It is the process when the pattern is transferred onto the substrate [18]. This pattern is formed from a photosensitive material (polymer) photoresist and involves several technological steps [19]. First, as depicted in Fig. 8, the samples are spin-coated with photoresist.

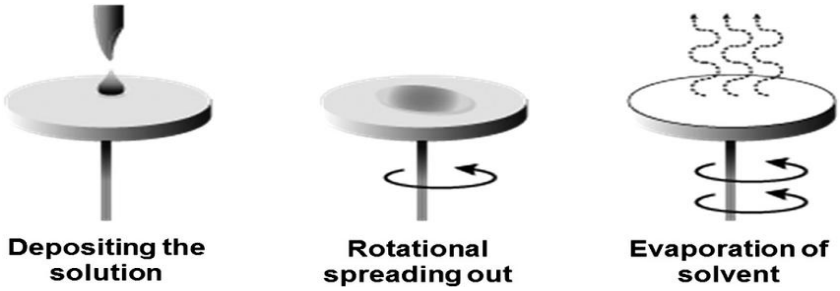

Fig. 8. Spin coating processes of thin-films [20].

Spin coating is a method used to deposit uniform thin films onto the substrates. Usually, a small amount of coating material is applied on the center of the substrate, which is not spinning. The substrate is then rotated at high speed (rotation speed of several 1000 revolutions per minute (rpm)) to spread the coating material by centrifugal force. The thickness of the layer depends on interaction between substrate and solvent (hydrophilic or hydrophobic), solution concentration, acceleration and velocity of spinning, solution evaporation rate, and spinning time. During the evaporation phase, the solution turns into a gel, because amount of the solvent constantly reduces and the viscosity increases. The rotation lasts 10-30 sec. It is fast technique forming uniform layers, but some defects onto substrate may occur, such as comets (Fig. 9a) (occurs when relatively large particles are present in the solution or on the substrate), stripes (Fig. 9b) (the variations in thickness during spinning of the substrate) or environmental defects (there must not be any changes of humidity level in the cleanroom).

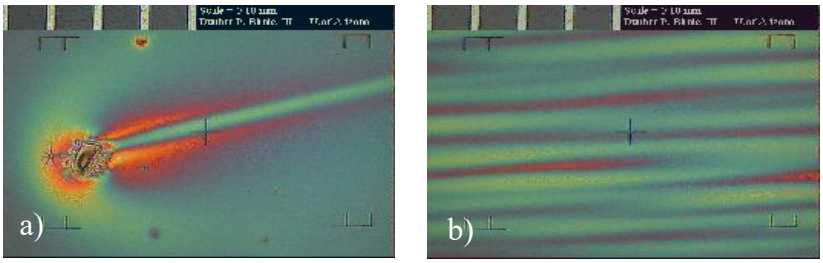

Fig. 9. Spin coating defects onto the photoresist: a) comet and b) stripes [21].

After coating, the resist film typically contains a residual solvent concentration of 10-35 % [22], which means that the wafer must be sufficiently dried for subsequent processing. This process, known as soft-bake, aims to lower the residual solvent concentration to avoid resist contamination of the photomask and to improve the resist adhesion to the substrate.

Thereafter, the coated substrate is partially illuminated with UV light. Three characteristic emission wavelengths from mercury vapor lamps are frequently used in photolithography: G-line (436 nm), H-line (405 nm), and I-line (365 nm) [22]. The wavelength of light used to determine the

minimum feature size that can be formed in the photoresist [23]. In unique instances, the implementation of extreme ultraviolet (EUV) lithography, with a range of 13.5 nm, can produce a resolution of 8 nm [24].

There are two ways in which the pattern can be transferred to the substrate. First is to illuminate the surface of the sample through a photomask on which the desired pattern has already been formed. It blocks or transmits UV light. Second - the surface is illuminated with a laser beam, which directly forms pattern. Exposed to light, the photoresist changes its chemical properties, so when the sample is immersed in the developer, the illuminated (or non-illuminated, depending on the type of photoresist) areas of the photoresist dissolve in it. The resulting pattern acts as a protective layer and can be used for etching or deposition of additional materials [25]. The type of photolithography depends on what type of photoresist is used. There could be positive, negative and image reversal photoresist as shown in Fig. 10.

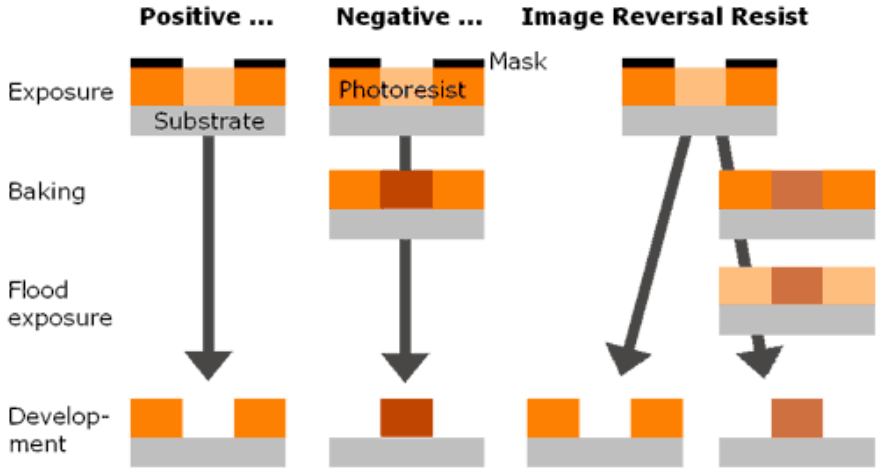

Fig. 10. Positive, negative, and image reversal resists for photolithography and their processing path [22].

Where the exposed areas are soluble in the developer and unexposed resist areas remain on substrate, it is called positive photolithography. Contrary, negative resists cross-link at high temperature after exposure and the exposed regions become less soluble, and the patterns formed in the negative resist are the reverse of the mask patterns [26]. While negative photoresist can be processed only negatively, the image reversal photoresist can be used for positive and negative photolithography. In positive mode, the process is the same as in positive photolithography, while in image reversal negative mode additional baking and flood exposure process steps are required, which render the first exposed areas insoluble in the developer and then make the areas that have not yet been exposed able to be developed. In addition, image reversal resist structures are less thermally and chemically stable than negative resist, but at the same time image reversal is better for lift-off process as it creates negative slope of photoresist [22].

1.5. Fabrication: profile control and dry etching

The ridge depth and sidewall profile in semiconductor structures are defined by the etching process. Etching profiles are commonly classified as isotropic or anisotropic, depending on the directionality of material removal. In isotropic etching, the etch rate is approximately same in all directions. As a result, material is removed both vertically and laterally, often producing rounded profiles and undercutting beneath the mask (Fig. 11a). This behavior is usually associated with diffusion-controlled processes, where the overall etch rate is limited by the transport of reactants to the surface and reaction products away from it [27].

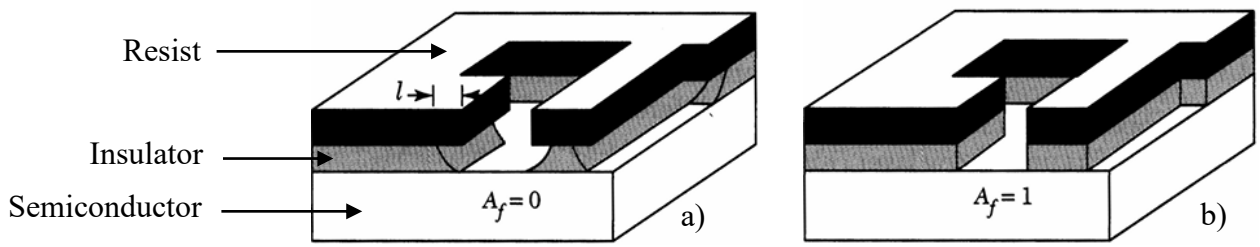

Fig. 11. Chemical etching profiles: a) isotropic and b) anisotropic [28].

In contrast, anisotropic etching occurs when material removal is direction-dependent. This produces more vertical sidewalls (Fig. 11) and allows better control of the etched profile, which is especially important for high-aspect-ratio structures and precise pattern transfer. As electronic devices and quantum structures decrease in size to the nanometer scale, it is crucial to produce anisotropic etching profiles with good uniformity. Anisotropy may result either from crystallographic effects, where different crystal planes etch at different rates, or from directional ion bombardment in dry plasma-based processes [29]. Thus, the most frequently used dry-etching technique is the reactive ion etching (RIE).

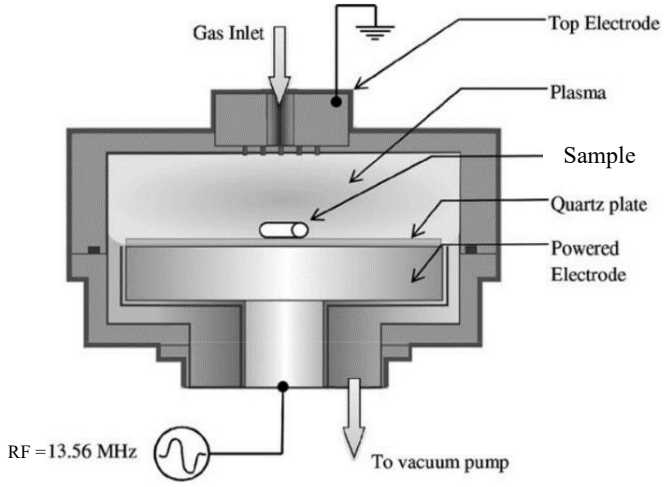

Fig. 12. Schematic diagram of the experimental setup for reactive ion etching process [30].

RIE uses a combination of chemical and physical reactions to remove material from the substrate. A power source that operates at radio frequency (RF) is employed to produce plasma and accelerate the entry of the ions into the wafer as depicted in Fig. 12. [27]. During the process electric field ionizes gas molecules creating radicals which cause chemical etching. At the same time free

electrons build up on sample surface creating electric field between positively charged plasma and negatively charged sample surface. Positive ions are accelerated towards sample and causes ion bombardment of sample surface. The ratio between chemical and physical reaction rates determines the slope of the etched sidewall. Isotropic etching is achieved when chemical process dominates and in contrary strong ion bombardment causes anisotropic process. By controlling process parameters such as gas composition and chamber pressure, RF power and substrate temperature the etching profile can be tailored from isotropic to highly anisotropic [31]. When dielectric material is etched using RIE, vertical profiles are achieved by sidewall passivation, typically by introducing a carbon-containing fluorine species (CHF_3 or CF_4/H_2) to the plasma [26]. Deep reactive ion etching (DRIE), which employ dual power sources – inductively coupled plasma (ICP) and capacitively coupled plasma (CCP) – is even more dependent on passivation to enhance anisotropy. Adjustment of the SF_6/O_2 ratio is commonly used to control passivation layer thickness and sidewall angle [31]. The silicon etch rate is primarily influenced by the SF_6 flow rate and ICP power, while the etch rate of masking materials depends on ion energy controlled by the CCP source [31]. For silicon etching, fluorine-based gases such as CF_4, CHF_3, and $C4F_8$, sometimes mixed with O_2, are commonly used. Fluorine reacts with silicon or silicon dioxide to form volatile SiF_4, which is removed under vacuum [32]. Anisotropic etching is achieved by ion bombardment at the bottom of the features, which removes reaction products and breaks Si–Si and Si–O bonds, which is shown in reaction below:

$$SiO_2 + 4F \rightarrow SiF_4 + O_2 \quad (3)$$

The major drawback of dry-etch processing is the deterioration of electronic characteristics, attributed to both mechanical displacement damage and charge-induced lattice damage due to ion bombardment.

1.6. Fabrication: hard-mask technology

When the photoresist is not durable enough for deep substrate etching, a hard mask is required. The choice of hard mask material depends on the substrate, device structure and fabrication technique. However, a key requirement is high selectivity, defined as the ratio of the mask etch rate to the substrate etch rate. Compared to photoresists, hard masks tolerate a wider temperature range and are less prone to cracking due to a closer match between their coefficients of thermal expansion and those of silicon [33]. Metals such as chromium, aluminum, nickel and titanium can be used as hard masks for the dry etching of SiO_2 [34]. Chromium is frequently used as a hard mask material due to its high-etch selectivity, low sputter yield, and good resistance to ion bombardment in fluorine-based plasmas [35]. Pattern transfer from the resist structure into Cr can be achieved either by lift-off or by employing the resist as an etching mask. However, SiO_2 is the most used hard mask material, thanks to its well-characterized material properties and mature growth, deposition, and etching processes [31]. Following lithography, the SiO_2 layer is etched and the photoresist is removed, leaving the

patterned SiO_2 to act as the etch mask. The thickness of this dielectric mask typically is in the range of 100–200 nm. Thicker masks enable deeper etching, while thinner masks allow the use of thinner resists and higher pattern resolution [36].

1.7. Fabrication: deposition techniques for semiconductor devices

The dielectric layer is a crucial component of the QCL fabrication process. This is an insulator layer that prevents electric current from passing through it. One of the frequently employed techniques for depositing dielectrics is plasma enhanced chemical vapour deposition (PECVD). It is a method of dielectric deposition using low deposition temperatures and RF to create plasma dissociation of gaseous precursors for acceleration of the chemical reactions. Schematic diagram is shown in Fig. 13.

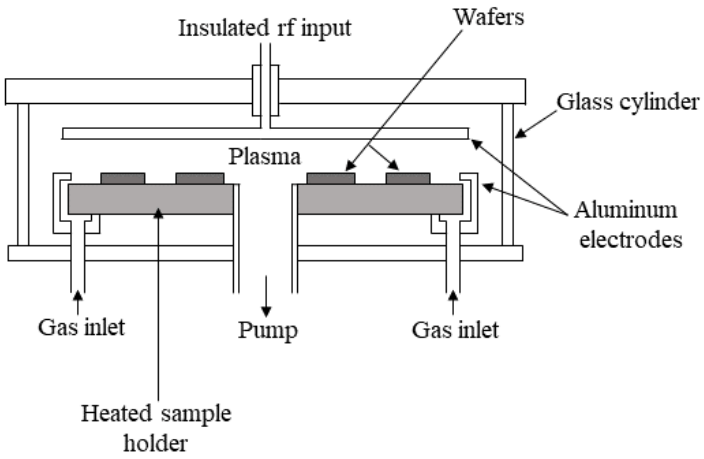

Fig. 13. Parallel-plate plasma deposition scheme (adapted) [26].

The wafer is placed in the aluminum deposition chamber between two parallel aluminum electrodes - a grounded electrode and usually an RF upper electrode. During the SiN deposition process, RF voltage is applied to generate a plasma discharge between those electrodes, while the substrate is typically heated to 100–400 °C [26]. Precursor gases such as silane (SiH_4) and ammonia (NH_3) are mixed with inert gases, including argon (Ar) or nitrogen (N_2) [37]. As a result, in an Ar plasma environment, SiH_4 and NH_3 react to form silicon nitride (SiN), as shown in the reaction:

$$SiH_4 + NH_3 \xrightarrow{300℃} SiNH + 3H_2 \quad (4)$$

These gases are introduced into the chamber via a shower head fixture over the substrate that helps to spread the gas more evenly onto the substrate. Chemical reactions first occur in the plasma because of precursor gas molecules colliding with highly energized electrons which then, via gas flow, travel to the substrate where they react and are adsorbed on the substrate surface to grow films. The chemical bi-products are then desorbed and pumped away, completing the deposition process [38]. One of the most used dielectrics is SiN. SiN_x is an outstanding electrical insulator and diffusion barrier against sodium and water vapour [39]. It has become a common replacement for CVD oxides in numerous

semiconductor devices due to its superior chemical resistance to acids, bases, salts, and molten metals [39]. It also exhibits a higher dielectric constant (k = 6 - 7) than silicon dioxide (SiO_2 - $k \approx 3.9$) [26].

Another deposition technique is magnetron sputtering - physical vapour deposition (PVD) method used to produce thin films and coatings under vacuum conditions. Fig. 14 illustrates schematic magnetron sputtering technique. During direct current magnetron sputtering, an electric field is established between the anode and cathode within a low-pressure inert gas atmosphere. The cathode, which is the sputtering target, deposits material onto the sample. Under the influence of the electric field, electrons accelerate towards the anode, ionizing the gas atoms upon collision. Once sufficient ionization has occurred, a glowing discharge - plasma, is formed. Positively charged ions are accelerated towards the cathode, bombarding the target and knocking out its atoms. These atoms are then deposited on the surface of the sample. To increase the impact energy, inert gases with a high atomic mass, such as argon or xenon, are used. During these collisions, secondary electrons are also knocked out and contribute to maintaining plasma. Sputtering efficiency is improved by placing a permanent magnet behind the target, creating a magnetic field parallel to its surface. This field traps electrons near the target, increasing plasma density and, consequently, the ion flux and deposition rate.

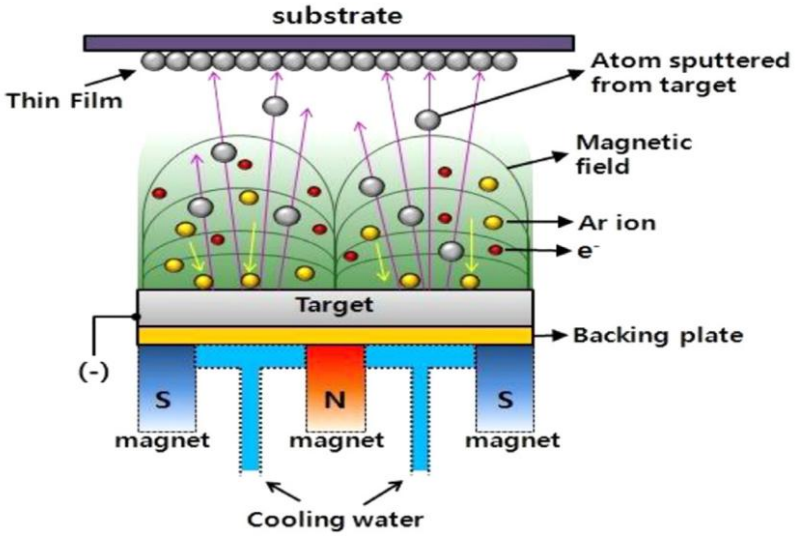

Fig. 14. Schematic magnetron sputtering deposition technique [40].

However, conventional DC magnetron sputtering is not suitable for depositing insulating materials, such as oxides, nitrides or ceramics, due to charge accumulation on the target surface. This screens the electric field, making it difficult to maintain the plasma. RF magnetron sputtering is used to solve this problem, where an alternating voltage of 13.56 MHz is applied between the electrodes. In this case, light electrons follow the changing electric field while heavy ions remain practically stationary. This causes the target to acquire a negative self-bias. Consequently, plasma ions are attracted to the target and bombard them, in a manner like that observed in the DC magnetron sputtering process [40], [41], [42].

2. Experimental methodology

2.1. Samples

The semiconductor structure VIA0028 QCL and QCD were grown using molecular beam epitaxy at the Department of Optoelectronics of the Center for Physical Sciences and Technology. A schematic representation of the epitaxial layer structure is provided in Fig. 15. The structure is grown on a n-type Si-doped InAs substrate. An n-type Si-doped InAs cladding layer is then grown, which has a lower refractive index compared to the active region, serving to confine the optical mode. Also, low doped InAs spacer around the active zone were formed to improve carrier mobility and optical gain. The active region, comprising 35 repeats of active quantum wells and injector/extractor structures designed for active electron transition at energies corresponding desired 8.4 μm emission wavelength. The thickness of the quantum wells determines the emission wavelength of the QCL. The active region is followed by another InAs spacer layer, and finally, an n-type Si-doped InAs cladding layer on top. The active region is where optical gain occurs through intersubband electron transitions. Thus, this work involved the processing of three VIA0028: 1, 2 and 3 samples that had the same heterostructure but differed only in the processing steps.

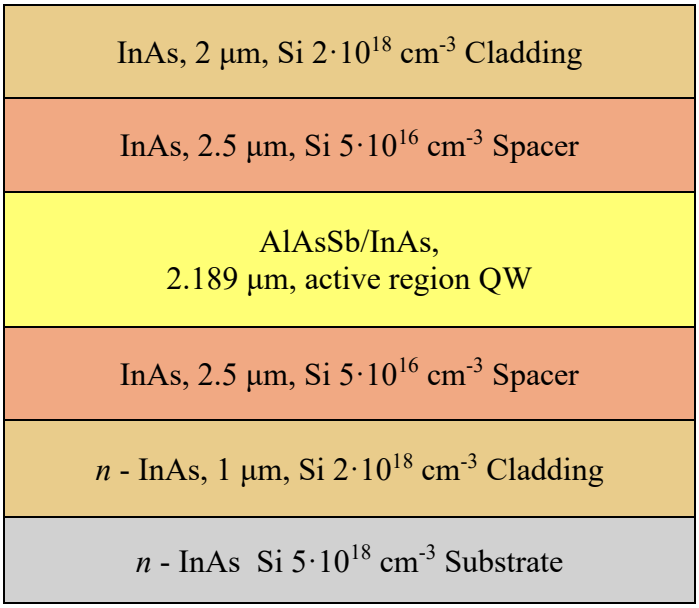

Fig. 15. Schematic representation of InAs/AlAsSb QCL and QCD structure.

2.2. Cleaning of the samples

Sample cleaning was carried out using an O_2 Diener Pico asher for 10 minutes. Additionally, an O_2 cleaning process was carried out in the Oxford Instruments PlasmaPro 80 RIE system prior to every dry etching step, for 1–3 minutes depending on the circumstances. The $NH_4 + H_2O$ solution at a ratio of 1:10 was used for oxide removal for 1 minute. In addition, before dry etching the semiconductor substrate, a 1:10 $HCl + H_2O$ solution was used for 1 minute.

2.3. Deposition of SiO_2

SiO_2 dielectric layers were deposited on InAs/AlAsSb epitaxial heterostructures via plasma-enhanced chemical vapour deposition (PECVD). Before deposition, the samples were cleaned in an NH_4-based plasma for 3 minutes at a power of 40 W, with a gas flow of 40 sccm, a pressure of 1 Torr and a temperature of 300 °C. SiO_2 deposition was carried out for 21 minutes and 4 seconds under the following conditions: SiH_4 flow rate of 6 sccm, N_2O flow rate of 710 sccm and Ar flow rate of 490 sccm. The chamber pressure was maintained at 1 Torr, the plasma power at 20 W and the substrate temperature at 300 °C. The thickness of dielectric layer was measured using an interferometer and it was 1190 nm (~1.2 μm).

2.4. Deposition of SiN

After the ridge formation, the sample was coated with an insulating layer of SiN using Oxfords instruments PlasmaPro 80 PECVD. Deposition duration was t = 30 min 20 s, with following conditions: Ar flow rate of 980 sccm, NH_3 flow rate of 30 sccm and SiH_4 flow rate of 12 sccm. The pressure was maintained at 1250 mTorr, the power at 10 W and the substrate temperature at 225 °C.

2.5. Photolithography

Firstly, the InAs/AlAsSb wafer was dipped in acetone for 10 minutes and rinsed in acetone and isopropyl alcohol (IPA) to remove organic contaminations. After Cr deposition, wafer was cleaned again and then annealed at T = 120 °C for 10 min to remove moisture from the surface. After annealing, positive photolithography was performed. The sample was coated with AZ1518 positive photoresist by SUSS LabCluster spin-coater centrifugation of speed 5000 rpm for t = 30 s and dried on a hotplate at T = 100 °C for t = 50 s. The wafer with the applied and cured photoresist was placed on the DWL 66+ (Heidelberg Instruments) and exposed to radiation at a wavelength of 405 nm with the estimated laser power 35 mW. For SiN etching, positive photolithography was performed again in two sequential exposure and dry etching cycles. Double layer of image-reversal photoresist Ti35E by centrifugation of 4000 rpm for t = 30 s and dried on a hotplate at T = 95 °C for 2 min was used. In the first cycle, SiN from the detector and ridge mirrors were defined using a laser exposure power of 200 mW. In the second cycle, only the lines for top electrodes were patterned, with the same laser power of 200 mW. When doing positive photolithography, the photoresist was developed immediately and the areas of the resist which have been exposed with laser light become soluble in the developer. For metallization, image-reverse photolithography was implemented, double layer of Ti35E photoresist at a centrifuge speed of 4000 rpm for 30 seconds is used as well. It is annealed at 95 °C for 2 minutes and exposed with laser lithography power of 220 mW. When photoresist is exposed to laser, chemical reactions take place within it, resulting in the release of nitrogen gas (N_2). These bubbles escape from a layer of photoresist of this thickness in approximately 10 minutes. While the photoresist was being degassed, the Mask Aligner SUSS MA/BA6 Gen 4 was prepared. Then sample

was annealed again at 120 °C for 2 minutes and it is called the reverse bake. As a result of this annealing process, the areas of the photoresist that were exposed to the laser become less sensitive to light. Afterwards, the entire sample is illuminated by UV radiation with 1040 mJ/cm^2 dose, causing the areas of the photoresist that were not exposed to the UV radiation in the first exposure to become soluble in the developer solution. Following the illumination process, photoresists are developed in a mixture of AZ351B developer and water with a ratio of AZ351B to H_2O of 1:4. The developing process lasts for 3 min for positive and 4 min for image reverse and is terminated by immersing the sample into the water. The wafer was then inspected under the Carl - Zeiss optical microscope.

2.6. Dry etching of RIE

Dry etching of the SiO_2 layer was performed using an Oxford Instruments reactive ion etching (RIE) system. This step was needed for hard mask formation. The SiO_2 layer was etched using a mixture of CHF_3 (17 sccm) and Ar (33 sccm) gases at a radio frequency (RF) power of 110 W for 60 minutes. This etching time was selected to remove approximately 120% of the target thickness and ensure complete etching. The measured etch rate of SiO_2 was 24 nm/min.

The semiconductor layers were then etched with Oxford Instruments inductively coupled plasma (ICP) RIE using a BCl_3 plasma with a gas flow of 7.5 sccm and an ICP power of 1000 W, with an RF power of 100 W and helium as a carrier gas at a pressure of 10 Torr. After the semiconductor etching process, any residual oxide was removed using an additional RIE step.

SiN etching was also performed using RIE at a temperature of 225 °C for 5 min 53 s, employing a CHF_3/O_2 gas mixture (CHF_3: 50 sccm, O_2: 5 sccm), with an etch rate of 102 nm/min.

2.7. Magnetron sputtering

For hard mask: Cr layers were formed on top of InAs/AlAsSb/SiO_2 sample using DC AMOD (Angstrom Engineering) magnetron sputtering. Before device deposition, the Cr source material was cleaned by pre-deposition to ensure the purity of the deposited metal. Once stable sputtering conditions had been achieved, the samples were mounted on the holder and placed inside the vacuum chamber. The process was carried out in an argon gas atmosphere at a pressure of 14 mTorr, using a deposition power of P = 84 W (U = 255 V, I = 329 mA). The deposition time was selected based on a previous calibration and it was t = 833 s. The film was deposited while rotating the sample to improve thickness uniformity.

For metallization: Sample VIA0028-1 was processed using a VST Model TFDS–870 e-beam evaporator for metallization. Ti/Au layers with a total thickness of 200 nm were deposited on the top surface to create ohmic contacts with the InAs. On the substrate side, Ti/Au layers were deposited to form ohmic contacts with the n-type InAs. Sample VIA0028-3 undergo metallization using a magnetron sputtering technique. This process was carried out in an argon atmosphere at a pressure of 14 mTorr and gas flow 6 sccm. For the top metallization, a 10 nm thick molybdenum (Mo) layer was

first deposited in DC mode (I = 329 mA, U = 227 V). This was followed by the deposition of a 250 nm - thick gold layer in RF mode at a power of P = 62 W. For the bottom metallization, a 10 nm thick Mo layer was deposited, followed by a 100 nm thick gold layer deposited in RF mode at a power of P = 60 W.

2.8. Characterization of InAs/AlAsSb QCL

The wavelength and electrical-optical characteristics of the QCLs were measured using a custom-built setup shown in Fig. 16. This setup operated in a pulsed mode, where the laser was powered by short current pulses to prevent the structure from overheating. For these measurements, very short pulses with a duration of 20 ns were used. The electrical excitation was provided by a high-voltage AVTECH AVRZ-5W-B pulse generator. This versatile unit can generate pulses ranging from 12 ns to 10 µs with a rise time of less than 6 ns at voltages up to 500 V. The generator was configured to supply pulses of a selected frequency, amplitude, delay, and duration to the QCL. To make sure the load impedance matched the standard 50 Ω coaxial cables, a non-inductive 50 Ω resistor was connected in series with the laser diode. A Tektronix MDO3102 oscilloscope was used to monitor the device's electrical response, which includes its voltage and current. One channel measured the voltage across the laser diode, while a second channel measured the current using a fast inductive probe. This probe has a current-to-voltage conversion factor of 1:1 (1A → 1V), which means that the response of the current pulse can be measured on the oscilloscope as a voltage pulse and converted to current. To measure the radiation intensity, an external mercury cadmium telluride (HgCdTe/MCT) detector was used. The detector signal was connected to an SRS860 lock-in amplifier, which was synchronized with the pulse generator to accurately measure the pulsed optical signal. The emission wavelength of the QCLs was determined separately using a Vertex 80 FTIR spectrometer.

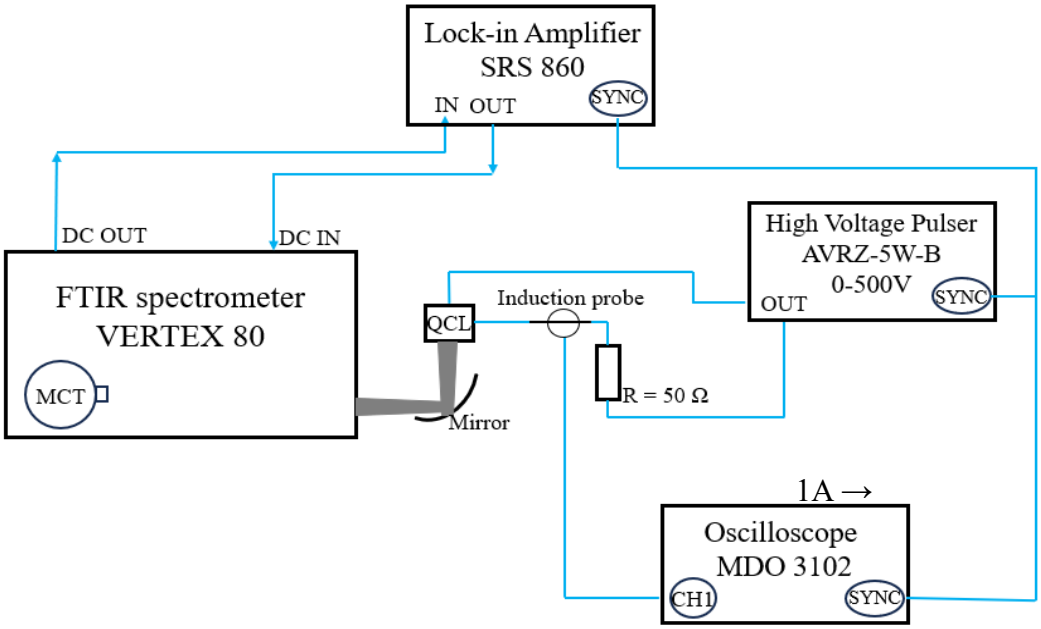

Fig. 16. Schematic drawing of the experimental setup for studying of electrical properties of QC devices.

3. Results and discussion

The results presented in this section focus on development of the fabrication process of monolithically integrated QCL and QCD, including the selection of appropriate mask materials and the adjustment of etching parameters to develop a robust hard mask suitable for deep etching. It was identified that maintaining a hard mask thickness of at least 1.2 μm formed out of SiO_2 is essential to withstand the subsequent deep dry etching of approximately 8 μm into the III–V semiconductor wafer. To achieve low surface roughness at the etched bottom, well-defined mirror facets, and smooth sidewalls, a series of technological experiments were performed. Additionally, particular attention was given to the geometric changes of the QCL, minimization of residual contamination on the sample surface and refining the metallization process.

All structures were fabricated in the Center for Physical Science and Technology at the Department of Physical Technologies. All technological steps are performed in cleanroom area.

3.1. Hard Mask Development and implementation

The fabrication of a reliable hard mask was a critical step for enabling deep dry etching (~8 μm) into the III–V semiconductor structure. Initial experiments showed that a SiO_2 layer of at least 1.2 μm thickness is required to withstand the etching process while preserving pattern fidelity. However, achieving smooth sidewalls and a low-roughness etched surface strongly depended on both mask material selection and process conditions. For this purpose, hard mask tests were initially performed on GaAs substrates instead of InAs/AlAsSb structures, because MBE growth of InAs/AlAsSb heterostructures is costly and limited, while many optimization experiments were required. GaAs was selected as a representative III–V arsenide material for preliminary process development since both GaAs and InAs are compatible with chlorine-based plasma etching chemistries.

At first, photoresist was investigated as a soft mask for pattern transfer into the SiO_2 layer. Positive photoresist AZ ECI 3012 provided good lithographic resolution and sufficient etch selectivity (~2.4:1), however during dry etching process the edge waviness occurs, as could be seen in Fig. 17, because of the standing wave interference during exposure. This effect led to non-uniform resist sidewalls, which were subsequently transferred into SiO_2 and underlying GaAs during etching.

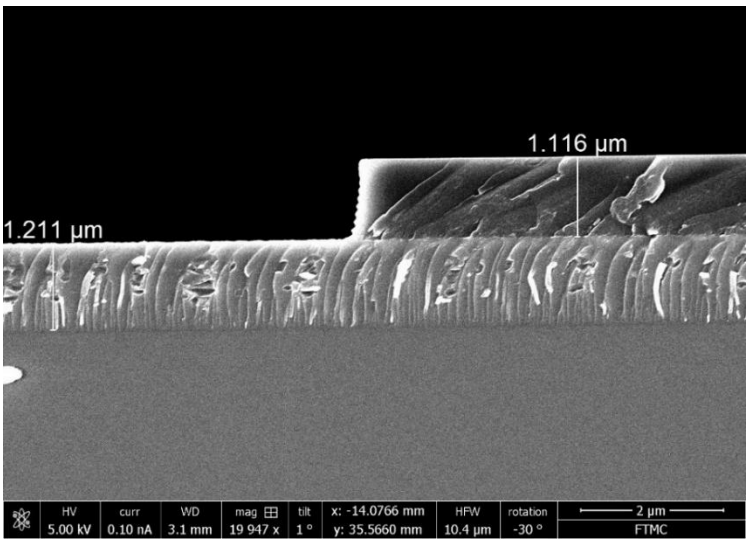

Fig. 17. SEM image of GaAs/SiO_2 substrate with structure formed from AZ ECI 3012 photoresist.

To mitigate this, a bottom antireflective layer (BARLi) was used. Since BARLi leaves residues in exposed areas additional O_2 plasma cleaning was introduced. This O_2 plasma cleaning caused significant thinning of the photoresist, leading to its complete removal during the subsequent SiO_2 dry etching step. As a result, previously unexposed SiO_2 areas became exposed and hard mask was additionally etched. Thinning of several hundred nanometers was observed. The remaining thickness was not suitable for further processing. Additionally, as seen in Fig. 18 rounded mask edges and insufficiently steep sidewalls were obtained, indicating poor pattern transfer.

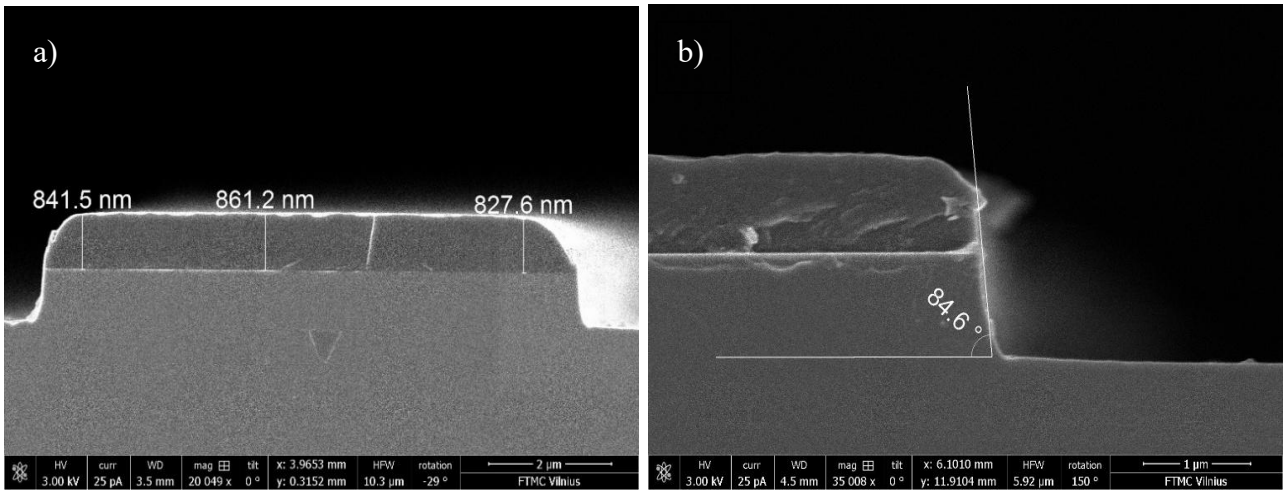

Fig. 18. SEM images of etched GaAs structure: a) thinning and rounding of SiO_2 layer and b) sidewall steepness.

Further experiments using thicker photoresist (AZ1518 – 1.8 µm thick) revealed thermal instability during reactive ion etching (RIE). Ion bombardment caused heating, leading to resist reflow and deformation of masked edges (see Fig. 19). This not only degraded feature definition but also complicated resist removal due to thermal hardening.

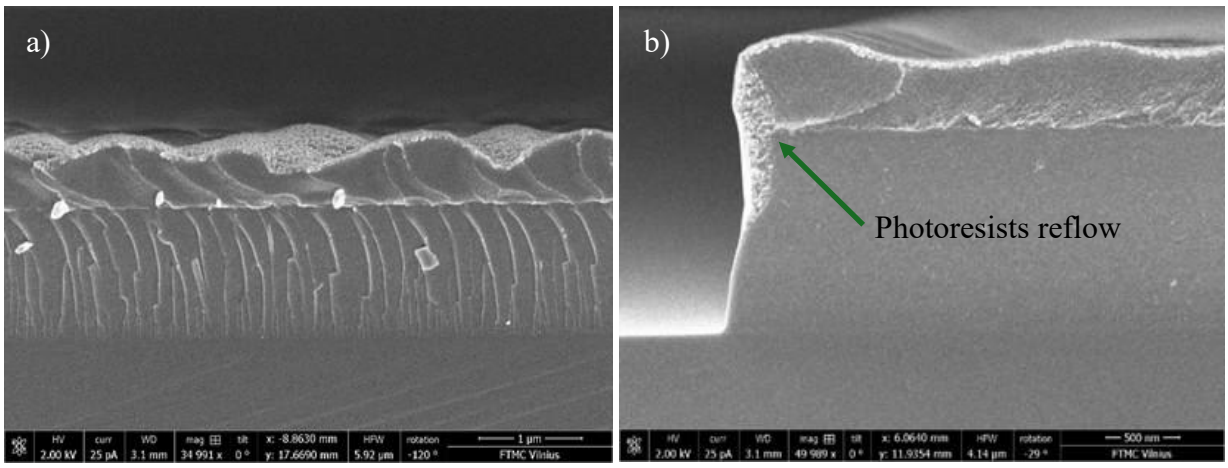

Fig. 19. SEM images of a) thermally damaged photoresist and b) defect of a sidewall caused by it reflow.

These findings demonstrated that photoresist-based masks are unsuitable for hard mask formation due to their limited thermal and etch resistance. Consequently, the fabrication of the mask shifted toward metal-based hard masks.

Chromium (Cr) was selected as a hard mask material due to its high resistance to plasma etching. Based on etch rate estimates of 1 nm/min for Cr and 24 nm/min for SiO_2, it was determined that a 100 nm thick Cr layer would be sufficient for pattern transfer into SiO_2. However, after the experiment, peak to peak surface roughness up to 500 nm was observed. To identify the type of residues present, the samples underwent two additional etching steps in RIE, using standard power (P = 110 W) for 15 minutes each time. AFM measurements were taken after each step, and it was found that the particle height decreased after each etching step, while the width remained almost unchanged and this could be seen in Fig. 20.

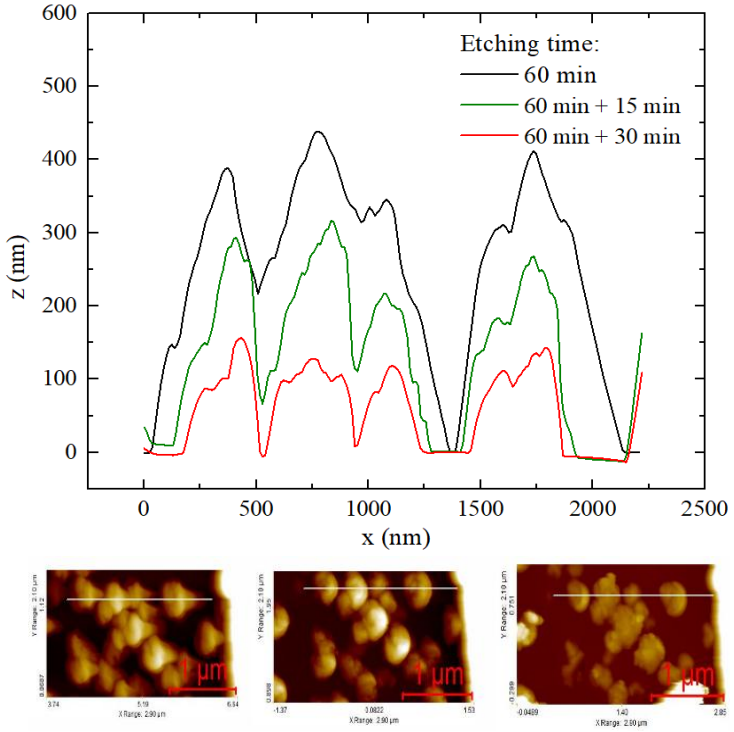

Fig. 20. AFM profiles after Cr etching with additional dry etching steps.

As the residues were gradually removed by the SiO_2 etching process, it could be concluded that the roughness of the sample was caused by SiO_2. It is thought that the residues were caused by Cr micro-masking during the RIE process. During dry etching, the Cr layer was sputtered away and could redeposit on the surface, acting as a local mask. It is known from the literature that re-deposition can be mitigated by either reducing the RIE power to decrease Cr sputtering or increasing the power to continuously re-etch redeposited Cr from the surface [43]. When the sample was etched using standard RIE power, the surface exhibited noticeable roughness (see Fig. 21a). Thus, the micro-mask effect was reduced by increasing the RIE power to P = 150 W, which enhanced ion bombardment and improved the removal of residual particles from the etched surface. Sample surfaces became significantly smoother, as could be seen in Fig. 21b.

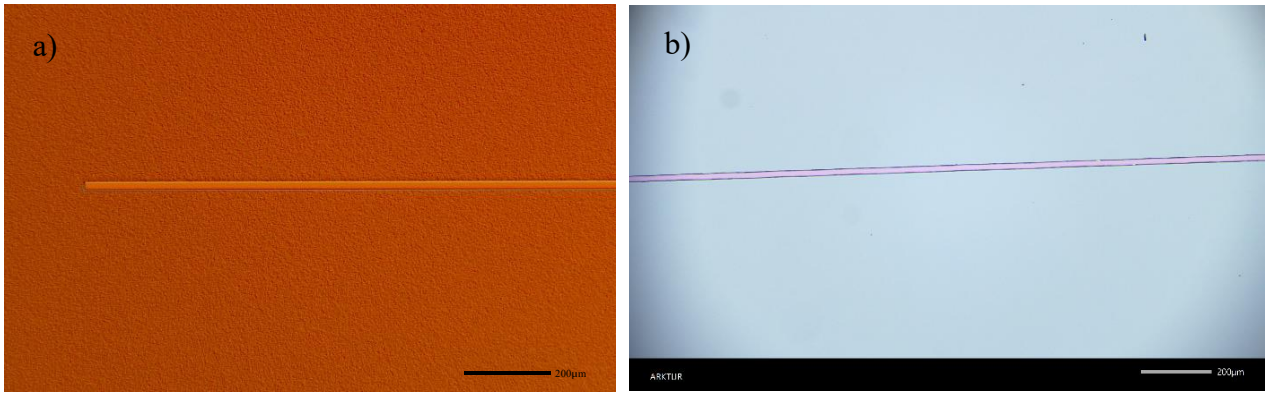

Fig. 21. Optical microscope images of Cr - GaAs/SiO_2 structure with a) rough surface after RIE with standard power (P = 110 W) and b) smooth surface with increased RIE power (P = 150 W).

3.2. Modification of the sample geometry

A monolithically integrated QCL-QCD photonic system was fabricated using an epitaxially grown InAs/AlAsSb (VIA0028) heterostructure. Three different configurations of QCL systems were fabricated: VIA0028 as epi-side up, VIA0028: 2 and 3 as epi-side down and epi-side down with metallized back mirrors. One of the device geometries depicted in Fig. 22.

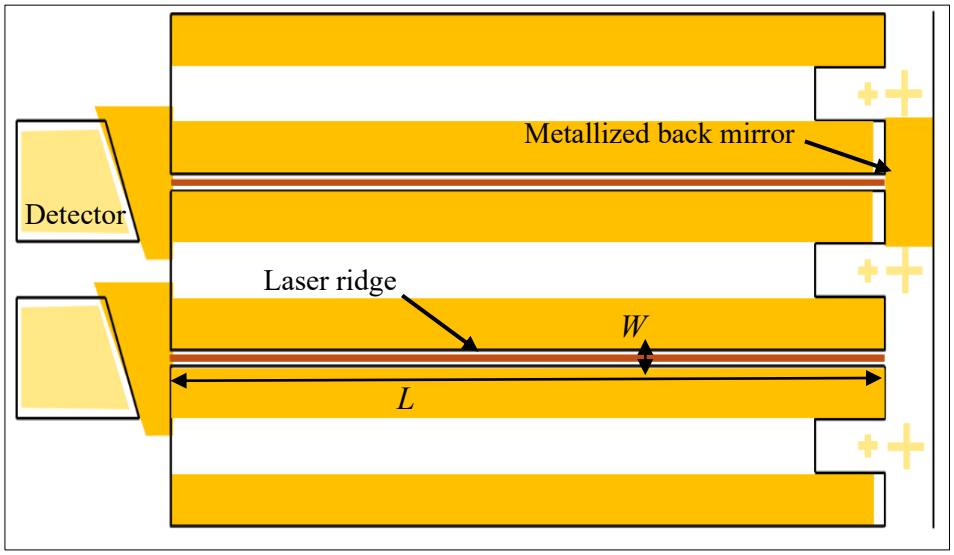

Fig. 22. Top-view layout schematic representation of epi-side down configurations device, where QCL cavity length denoted as L and ridge width - W.

The same geometrical parameters were used for all fabricated QCL-QCD configurations, including the epi-side up and epi-side down devices. The QCL cavity length was L_{QCL} = 3 mm, and the ridge width was W_{QCL} = 12.6 μm. The QCD detector area was S_{QCD} = 0.107 mm^2, and the detector itself was formed at the Brewster angle with respect to the QCL emission direction. The etching depth was d_{etch} = 10 μm, while the deposited SiN dielectric layer had a thickness of d_{SiN} = 500 nm. Thus, the fabricated devices had identical laser and detector geometries, while the differences between the configurations were related only to the mounting orientation.

As a result, VIA0028 – 1 was fabricated using an epi-side up mounting configuration, in which the laser chip is mounted with its substrate side attached to the heat sink. The epitaxial side, which contains the active region, faces upwards. In this configuration, the p-side/top contact is usually accessible from above, which makes processing and contacting less complicated. However, since the active region is positioned further from the heat sink, heat generated during device operation must be dissipated through a longer thermal path [44]. Consequently, epi-side up mounting generally results in less efficient heat removal than epi-side down mounting. Another issue was that electrical testing of the fabricated devices revealed that the QCLs were short-circuited. Inspection of SEM images indicates a possible presence of residual polymer contamination along the etched sidewalls of the processed structure (see in Fig. 23, green arrow). This may lead to unintended electrical pathways, which can result in short-circuit formation.

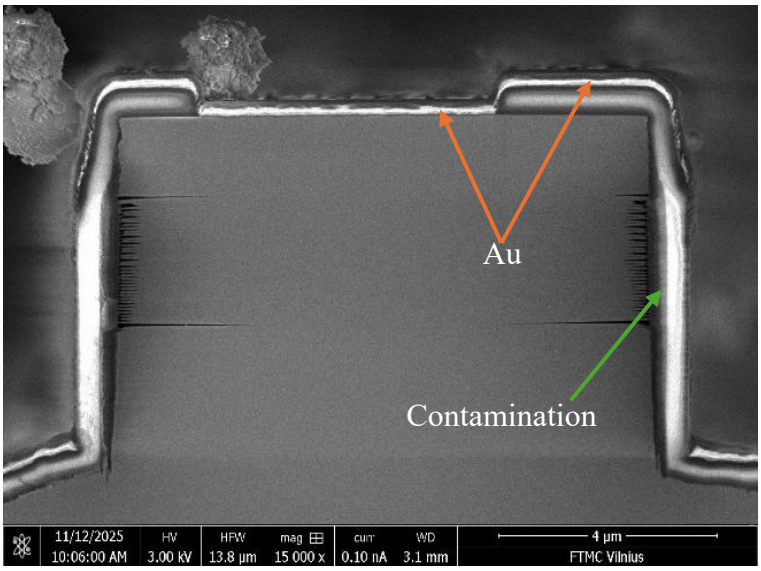

Fig. 23. SEM cross-section image of fabricated VIA0028-1 QCL ridge.

Based on these observations, the fabrication approach was reconsidered. To reduce the likelihood of sidewall-related contamination effects and improve processing reliability, VIA0028: 2 and 3 were fabricated using an epi-side down configuration. This device configuration was modified because relatively large areas of the epitaxial structure had to be etched in the epi-side up configuration. This increased the possibility that residual defects or micro-masking related features would remain on the etched surface. These local defects could lead to non-uniform SiN deposition,

which would thin the dielectric layer in certain areas. Consequently, the dielectric layer could not withstand the applied voltage during electrical measurements, which could result in a short circuit. Moreover, additional O_2 plasma cleaning steps were introduced after each dry etching step to completely prevent polymer residue formation. As a result, VIA0028-2 and VIA0028-3 were fabricated in epi-side down configuration, unfortunately VIA0028-2 devices were damaged during fabrication. Additionally, two of the five QCL structures in VIA0028-3 sample were fabricated with back mirrors coated in gold. Metallization of the back mirror lowers optical losses, which reduces the current needed for lasing threshold.

3.3. Two-cycle etching of SiN

During the processing of the VIA0028 QCL-QCD devices, several technological difficulties were encountered. One of these issues was inconsistent patterning during the SiN removal process: either the detector regions or the area for top electrodes were well defined, but not both. Optical microscope images show InAs/AlAsSb ridge structure after SiN removal (see Fig. 24). It can be seen that either the entire top area of the ridge or its edges are free from SiN, which could short circuit QCL structure. This inconsistent pattering was due to significant differences in photoresist thickness in the various areas. The photoresist layer thickness on top of the ridges was a few times thinner compared to the detector region.

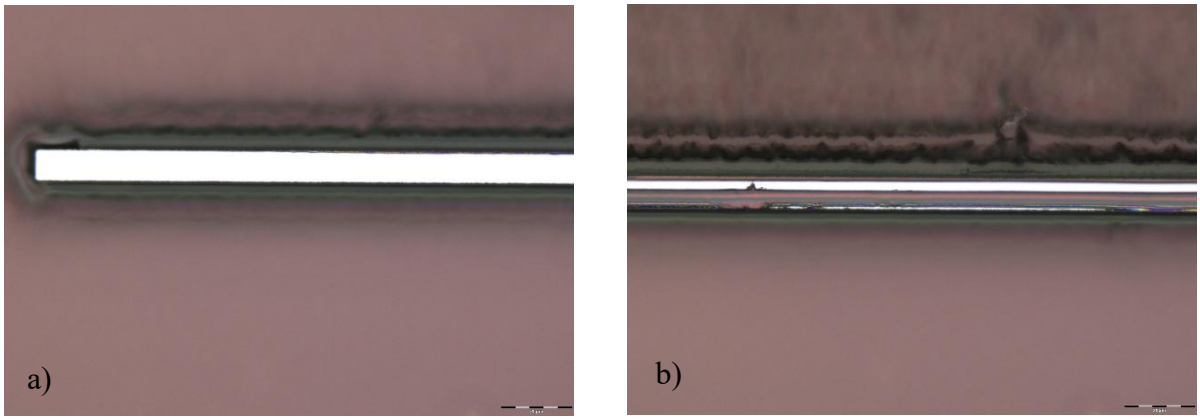

Fig. 24. Optical microscope images of VIA0028 QCL ridge after the SiN etching, where a) SiN are completely removed from the top area of the ridge and b) partially removed.

Therefore, a modified two cycle SiN removal process was introduced to improve pattern transfer and ensure complete opening of both the detector area and the narrow line regions. The SiN etching was performed in two separate steps. In the first step, the SiN layer was patterned and removed from the large area regions: detector areas and ridge mirror regions. In the second step, a separate photolithography and etching was carried out to open only the narrow lines for the top electrodes. Fig. 25 shows an optical microscope image of the processed structure after the modified two-step SiN etching. The detector and the narrow top electrode line regions are clearly formed, with well-defined edges and good alignment between the patterned features.

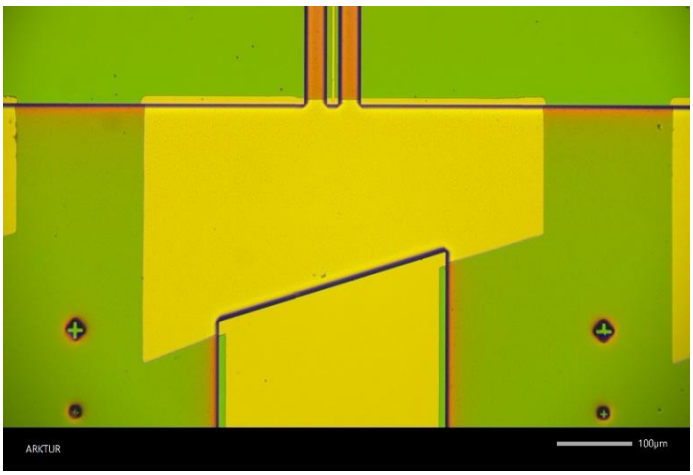

Fig. 25. Optical microscope image of VIA0028 QCL-QCD device after the two-step SiN etching.

3.4. Metallization

Top electrode for VIA0028–1 was fabricated using electron-beam (e-beam) deposition. However, metal layer did not uniformly cover all required areas. This could be seen from the previous SEM image depicted in Fig. 23, as thin gold metallization layer that is denoted with orange arrow, disappears from the sidewalls of the ridge. To prove that external electrodes were added to the contact pads on opposite sides of the ridge. No electrical continuity between these contact pads was measured.

For that reason, the deposition method for electrodes was subsequently changed to magnetron sputtering to improve film deposition on vertical sidewalls. VIA0028–3 contact formation were fabricated using magnetron sputtering. This approach was selected because the e-beam evaporation is a highly directional deposition technique, where the material is deposited from the source located below the sample. Consequently, the material mainly reaches the surface from one direction, which prevents the vertical sidewalls from being fully coated. In contrast, due to the configuration of magnetron sputtering machine the sputtering target is fixed at an angle. Therefore sputtered atoms can reach the vertical walls from various angles, including oblique ones. This reduces the shadowing effect by allowing the material to coat vertical ridge sidewalls more effectively, as shown in Fig. 26.

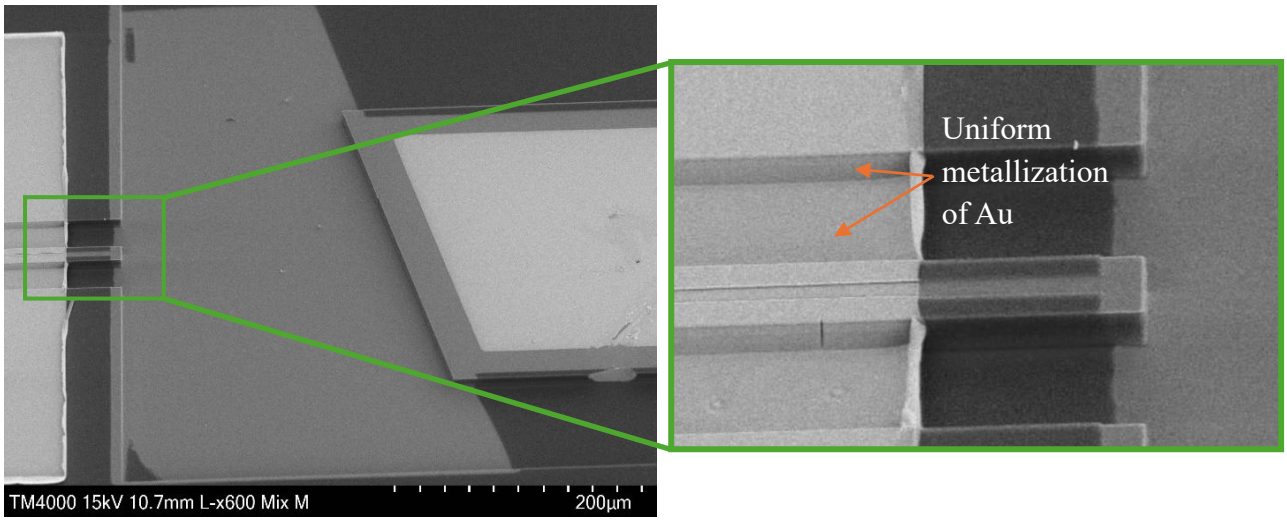

Fig. 26. SEM image of fabricated VIA0028-3 QCL, where metallization was performed by magnetron sputtering.

3.5. Investigation of surface materials

To verify the final InAs/AlAsSb device surface composition after the fabrication, energy-dispersive X-ray spectroscopy (EDX) was performed and plotted in Fig. 27. EDX allows elemental analysis by detecting characteristic X-rays emitted from the sample.

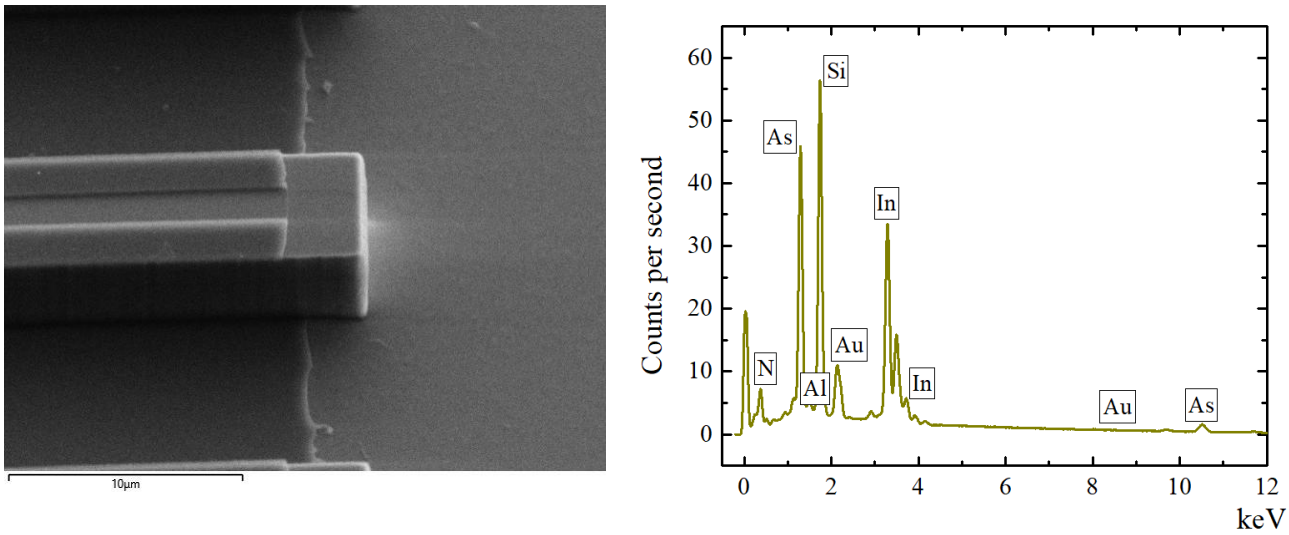

Fig. 27. SEM image of the fabricated InAs/AlAsSb QCL (left) and EDX spectrum (right).

The EDX results confirmed the presence of the expected elements, such as In, As, Si, and N. Indium and arsenic are attributed to the InAs substrate and the InAs/AlAsSb epitaxial structure, whereas silicon and nitrogen originate from the deposited SiN dielectric layer. However, from the EDX mapping, depicted in Fig. 28, a huge amount of N across the entire area could be seen.

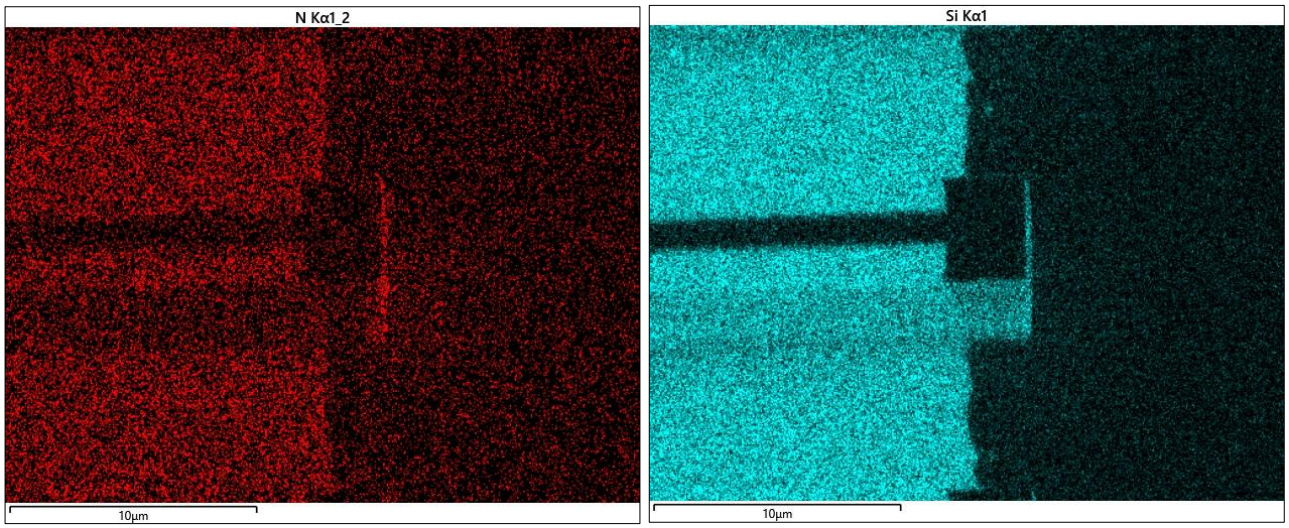

Fig. 28. EDX mapping images of N and Si on the fabricated QCL.

The nitrogen signal was most likely detected due to insufficiently high vacuum conditions during the EDX measurement. Under these conditions, residual nitrogen-containing gas in the SEM chamber can contribute to the background signal. Since N has a low-energy X-ray emission line (0.39 keV), the resulting EDX map shows a seemingly uniform distribution that does not necessarily represent the actual composition of the sample. Nevertheless, denser areas of N could be spotted on the ridge, indicating the presence of SiN.

Moreover, Fig. 28 reveals another important aspect: silicon presence on the sidewalls of the ridge. This suggests that Si was not completely removed during the dry etching process. According to the literature, incomplete SiN removal could lead to reduced optical power and thermal management and prevent high-quality electrical contact between the semiconductor material and the top metal contact. In some cases, the remaining SiN layer on the sidewalls may act as a transparent passivation layer, but its thickness must be determined in order to evaluate its influence on the device's optical and electrical properties.

Furthermore, from EDX spectrum (Fig. 27), a noticeable Au signal was detected in the ridge region, although gold in this area is absent. The signal is probably related to the SEM-EDX measurement conditions rather than the ridge's actual composition. Since EDX collects X-rays from a finite interaction volume, the detected signal may include contributions from nearby gold metallization or contact regions.

Additionally, measuring the finished device shows that no Cr remains on the surface, as the EDX peak for Cr is located at 5.4 keV [45]. This indicates that chromium redeposition was effectively eliminated during fabrication. The same applies to the other elements, used in RIE process such as bromine (Br), chlorine (Cl) and fluorine (F), which should correspond to 11.9 keV, 2.6 keV and 0.67 keV, respectively. [46].

3.6. Spectrum measurement results

The measured emission spectrum of the InAs/AlAsSb quantum cascade laser exhibits a single dominant peak, which is depicted in Fig. 29.

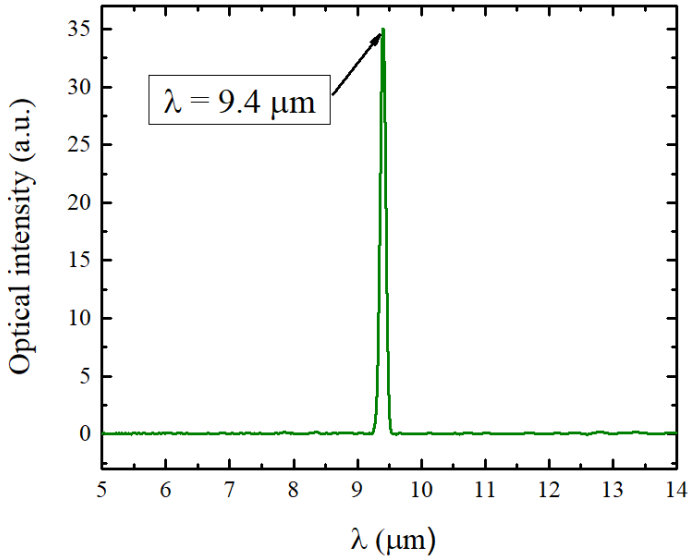

Fig. 29. Spectrum of fabricated VIA0028-3 QCL.

The measured emission spectrum showed a peak wavelength of approximately 9.4 μm, whereas the designed emission wavelength was around 8.4 μm. This shift indicates that the grown epitaxial structure did not fully match the intended design, which may be attributed to deviations in the growth process and needs to be inspected.

3.7. Electrical and optical measurement results

The *VI* characteristics of a fabricated VIA0028 – 3 InAs/AlAsSb QCLs are shown in the Fig. 30.

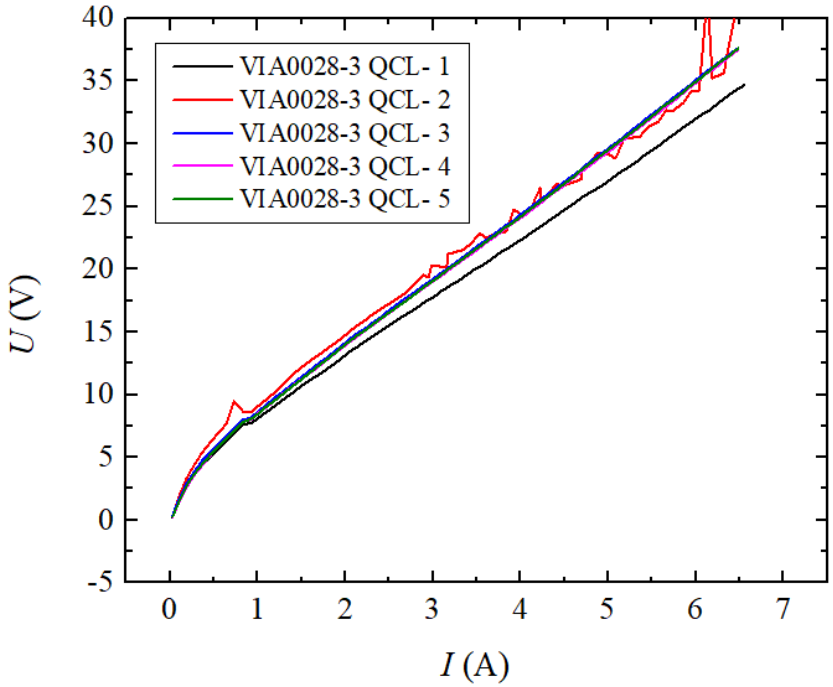

Fig. 30. InAs/AlAsSb QCLs voltage - current dependence curves.

The measured *VI* characteristics exhibit nonlinear behavior at low bias, near 0 V. For this type of structure, distinct threshold-like behaviour is typically expected, since a certain applied voltage is required to align the energy levels in the active region and enable efficient carrier transport. Ideally, at low voltage the current remains very small and the curve is almost flat, then after the turn-on voltage it bends upward and increases steeply and smoothly with applied voltage. In this case, the current of QCLs starts to increase gradually and the curve bends already at low voltage. This behavior suggests the presence of leakage current, most likely caused by shunt paths within the structure. One possible reason for this behavior is the absence of a hole-blocking layer, which would normally help confine charge carriers and reduce leakage. Without this layer, holes may overflow into adjacent regions, leading to increased non-radiative recombination and reduced device efficiency. However, after reaching the operating voltage range (around 6V), the *VI* curve becomes almost linear, indicating a nearly constant differential resistance.

Furthermore, the optical power versus current characteristics of fabricated InAs/AlAsSb QCLs are shown in Fig. 31. From *PI* characteristics, a slight difference in the threshold current (I_{th}) can be observed between the two different configurations of VIA0028 - 3 QCLs.

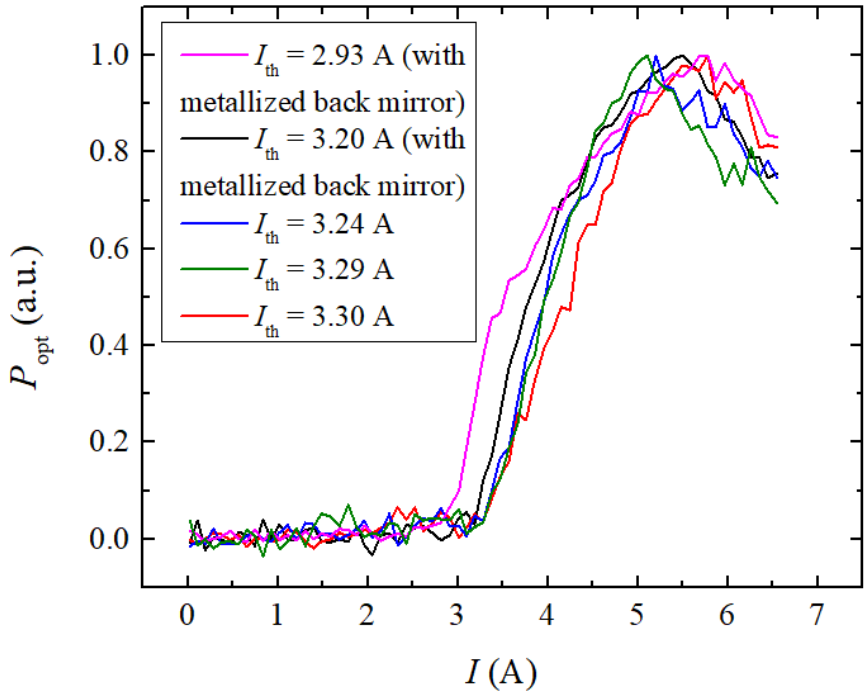

Fig. 31. InAs/AlAsSb QCLs optical power – current dependance plot.

At low injection currents optical power emitted by QCL is low and starts to increase abruptly from a certain current value. Therefore, spontaneous emission is observed up to a certain I_{th} and stimulated emission is observed when the threshold is reached. The optical output power of QCL was expected to increase approximately linearly with increasing current above the threshold current, I_{th}. However, as shown in Fig. 31, the output power reaches a maximum value and then starts to decrease for all devices. This behavior is known as thermal rollover and is typically caused by device heating at higher injection currents. As discussed in the previous section, additional effects such as a nonlinear shunt path across the laser or carrier overflow into the cladding layers may also contribute to the reduced performance [47].

In addition, the devices with the gold-plated back mirror (magenta and black curves) exhibit slightly lower threshold current compared to the device without gold plating. The back mirror metallization refers to the deposition of a high-reflectivity coating on the rear facet of the laser cavity. Its purpose is to increase optical feedback by reflecting more light back into the cavity and reducing optical losses through the back facet, such lowering threshold current density [48]. However, variation in I_{th} observed in the Fig. 31 for devices with a metallized back mirror suggests that the newly introduced configuration change was not fully developed, potentially introducing additional fabrication-related non-uniformities.

Therefore, to better compare the optical characteristics of the devices, the corresponding threshold current densities of VIA0028–3 QCLs were calculated by formula:

$$J = \frac{I_{th}}{W \cdot L}, \quad (5)$$

where I_{th} – threshold current, W – width of the ridge (W = 12.629 μm) and L – length of the cavity (L = 3 mm).

The calculated current densities for the QCLs with and without a metallized back mirror were around 7.73 kA/cm^2 and 8.68 kA/cm^2, respectively. Nevertheless, both values are still relatively high compared with optimized mid-infrared QCLs reported in the literature. For 10 μm with J_{th} = 3.2 kA/cm^2 at the maximum operation temperature T_{max} = 270 K [49], while more recent mid-infrared wavelength QCLs have demonstrated threshold current densities as low as J = 0.6 kA/cm^2 [50].

3.8. Challenges in quantum cascade detector measurement

The operation of the fabricated QCD could not be reliably confirmed using the current measurement setup. In the present configuration, it was not possible to measure the detector response while simultaneously driving the laser in a controlled optical measurement arrangement. Since the laser was operated using nanosecond step-like front current pulses, these fast electrical transients induce response in QCD. This response changes linearly with QCL supply voltage and is several orders of magnitude higher than expected voltage generated from optical response. Therefore, detecting optical signals is difficult. To avoid this effect, the laser could be operated in continuous wave mode, where the influence of pulsed electrical interference is reduced. However, CW operation was not achievable for the current samples due to insufficient heat dissipation. Further improvement would require better thermal management, for instance, by thinning the substrate and increasing the thickness of the top metallization to several or tens of micrometers to improve heat spreading and heat removal.

Conclusions

1. The QCL device was successfully fabricated using the developed main processing steps, and EDX analysis did not reveal significant processing-related residues, such as Cr, Br, Cl, or F, on the device surface.
2. Photoresist masks were unsuitable for SiO_2 etching because they degraded during RIE and caused uneven pattern edges, whereas Cr hard masks enabled reliable pattern transfer and better geometry control.
3. Anomalies in electrical and optical properties observed in QCL, such as high current densities (~8.68 kA/cm^2) may indicate carrier overflow into the cladding layers or current leakage through non-radiative paths.

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Santrauka (lietuvių kalba)

Vidutinio IR diapazono monolitinės fotoninės sistemos gamyba naudojant III-V puslaidininkius

Karina Pokaliuk

Šio darbo tikslas yra pagaminti monolitinę fotoninę III–V puslaidininkių medžiagų sistemą, sudarytą iš kvantinio kaskadinio lazerio (QCL) ir kvantinio kaskadinio detektoriaus (QCD). Tam ypač svarbu ištobulinti technologinio proceso žingsnius. QCL prietaisų geometrinė konfigūracija buvo pakeista iš epitaksiniu sluoksniu į viršų (angl. *epi-side up*) į epitaksiniu sluoksniu į apačią (angl. *epi-side down*). Tokiu būdu buvo sumažinti ėsdinami struktūros plotai ir sumažinta tikimybė, kad ant išėsdinto paviršiaus susidarys defektai arba mikromaskavimo sukelti dariniai. Kitas technologinio proceso etapas buvo 1,2 µm storio SiO_2 kietosios kaukės formavimas, reikalingam apie 8 µm gylio struktūroms InAs padėkle išėsdinti. Dėl šios priežasties buvo tiriamos skirtingos medžiagos, kurios galėtų veikti kaip apsauginė kaukė SiO_2 sluoksnio sauso ėsdinimo metu. Nustatyta, kad fotorezistas, naudojamas kaip minkštoji kaukė ant SiO_2 sluoksnio, nėra tinkamas storai kietai kaukei formuoti RIE metodu, nes susidaro vingiuoti kaukės kraštai, netolygus paviršius arba dėl intensyvaus jonų bombardavimo - išsilydo ir nuteka, dar labiau blogindamas struktūros geometriją. Kaip alternatyva buvo išbandyta chromo kietoji kaukė. Pastebėta, kad ėsdinant RIE metodu su standartine galia (P = 110 W) vyksta kietosios kaukės medžiagos pernešimas (re-deposition), dėl kurio ant struktūros dugno susidaro apie ~500 nm aukščio dariniai, o paviršius tampa šiurkštus ir matinis. Padidinus sausojo ėsdinimo galią (P = 150 W), šis efektas buvo pašalintas ir suformuotos statmenos struktūrų sienelės. Taip pat, SiN dielektriko ėsdinimas buvo pakeistas į dviejų žingsnių procesą. Dėl skirtingų detektoriaus ir viršutinių elektrodų linijų plotų fotolitografijos proceso metu susidarydavo nevienodas fotorezisto storis. Dėl šios priežasties SiN sluoksnis būdavo pašalinamas netolygiai: arba nuo visos viršutinės briaunos paviršiaus, arba tik nuo jos kraštų. Pakeistas ir metalizacijos procesas: vietoje elektronų pluošto garinimo buvo taikytas magnetroninis dulkinimas. Šis metodas leido užtikrinti tolygesnį metalo nusodinimą ant briauninės struktūros šoninių sienelių. Galiausiai, pagamintuose QCL prietaisuose, kurių lazeriavimo bangos ilgis buvo 9,4 µm, mažiausias slenkstinės srovės tankis siekė J = 7,76 kA/cm^2, esant I_{th} = 2,92 A slenkstinei srovei. Vis dėlto toks didelis srovės tankis rodo galimą srovės nutekėjimą arba krūvininkų pabėgimą į dengiamuosius sluoksnius (angl. *cladding layers*).