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MODELLING AND CHARACTERIZATION OF COMPONENTS FOR D-BAND COMMUNICATION FRONTEND

Master's final thesis
Electronics and Telecommunication Technologies study programme

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Table of contents

Introduction

The D-band (110–170 GHz) is recognized as a crucial spectrum for future 6G networks, offering substantial bandwidth for achieving ultra-high data rates, sometimes exceeding 100 Gbps [1][2].

To synthesize the necessary D-band signals, frequency multiplication is a preferred method, often relying on transistor-based frequency triplers [3] [5]. Transistor multipliers can achieve higher conversion gain compared to passive diode multipliers because they exploit the device's transconductance [10]. Advanced tripler implementations often utilize balanced topologies which inherently suppress unwanted odd-order harmonics, enabling broadband operation and cleaner spectral output [2] [3]. For instance, a two-stage design may incorporate a balanced tripler followed by a harmonic-rejection power amplifier to ensure spectral purity [3].

As an industry problem, demand for wireless fast data traffic urging the world to use and develop unused high frequency spectrum. D-band offers wide bandwidth and high speed like 100+ Gbps. However, to design such kind of elements is very challenging and requires considerations. For technical side of view, every elements need individual approach, as substrate coupling, impedance interactions, and bias dependencies connect these elements. And after this, the performance should be checked in overall system too. In the end, estimated results and real-world results should be compared to evaluate performance. [8]

In this work, frontend of D-band communication system modelled. The circuit and elements layouts are characterized and compared. Prototype chip has been produced and electrical characterization have been performed. The outline of this thesis is given as follows. Literature review for transmitter frontend for communication in D-band has presented in Chapter 1. In Chapter 2 the circuit, layout, substrate have been modelled and simulated in ADS software. Results have been shown compared and explained. Produced prototype chip have been showed and test results and comparison have been discussed in Chapter 3.

1. Introduction to D-Band Communications and Transmitter Frontends

1.1. Role of Millimeter Waves in technology

As 4G operates below 6 GHz that is considered low frequencies compared to new technologies, and these frequencies are very crowded. For that reason, 5G introduced millimeter waves (mmWave) which diversified the frequency array. 5G technology is huge improvement, but still new technologies and applications need more data. They demand high speed and almost zero latency. As example for these applications, Virtual Reality (VR), Internet of Things (IoT) and autonomous transportation can be mentioned. [9]

To support these statements ITU's "IMT traffic estimates for the years 2020 to 2030" report can be reviewed. [14] This report states the traffic increase yearly and what drives this demand. Also, estimation graphs have been presented in [14], as an example shown in below:

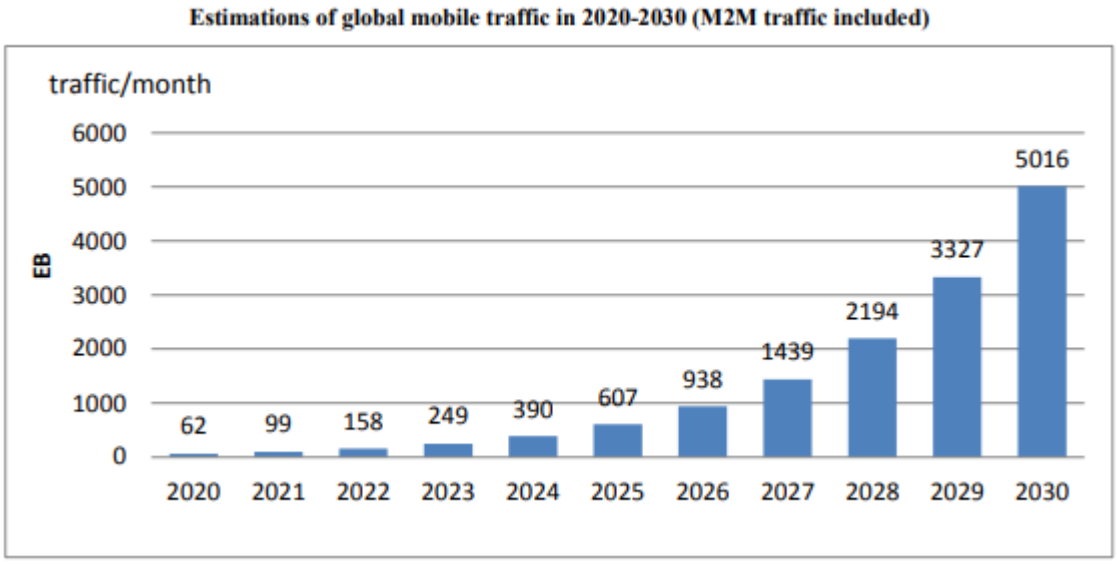

Fig. 1.1.1. The ITU's predicted exponential growth in mobile data traffic through 2030 [14]

To note, 1 Exabyte = 1 000 Petabytes = 1 000 000 Terabytes, so basically Exabyte equals to 10^{18} bytes.

In today's available mmWave band it very hard to acquire 100 Gbps, even to reach this speed equipments should be very perfect which is almost impossible. To get this kind fast data transmission it is needed to move higher frequencies, above 100 GHz. [9]

Let‘s look through figure to see electromagnetic spectrum and compare them. Just right after mmWaves and Terahertz (THz) there are visible light frequencies. They are very fast but have drawbacks, such as they are very sensitive sun light and fog, rain absorption. And after these frequencies UV, X-ray arrays come. But, these frequencies are harmful to human tissues as they can damage human DNA. [9]

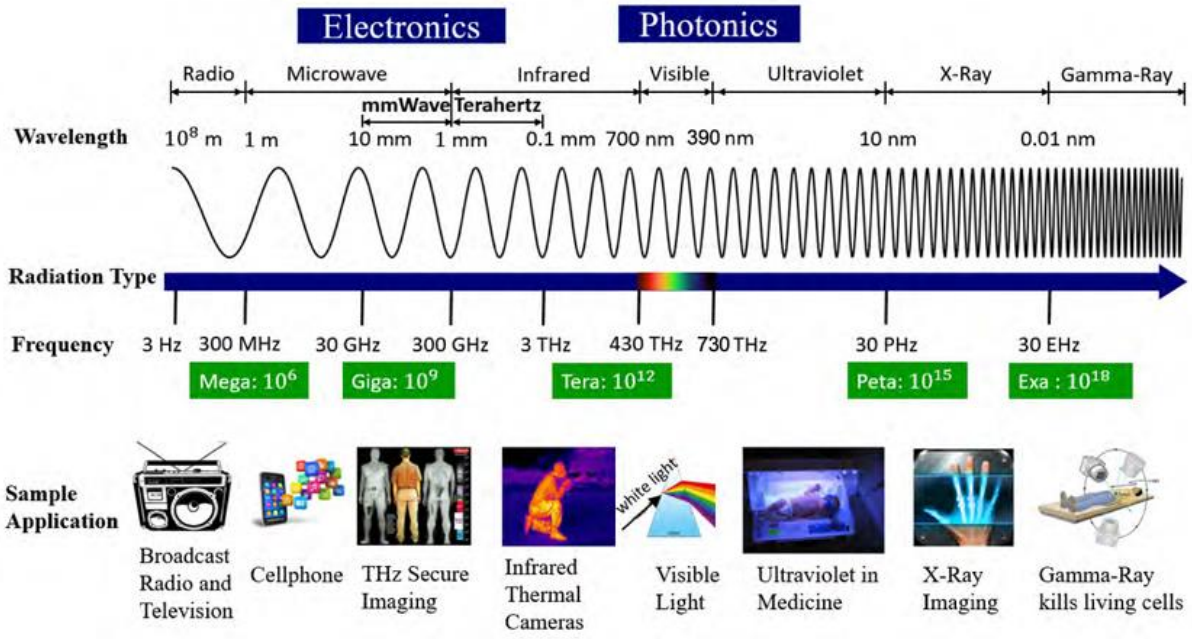

Fig. 1.1.2. Electromagnetic spectrum and applications [9]

1.2. D-Band’s (110-170 GHz) role in 6G and beyond

The concept of sixth-generation (6G) wireless telecommunication networks and other cutting-edge applications has made the D-band, which spans frequencies from 110 GHz to 170 GHz, a crucial spectral region. It is because D-band spectrum offers wide bandwidth that can handle higher data rates, more precisely higher than 100 Gbps [6]. Beside 6G technology, they are essential for imaging, data center’s wireless interconnection, and etc. Because these frequencies provide benefits like reduced latency, high-speed data transmission, and enhanced spatial resolution—all crucial for meeting the demands of industrial automation, long-range satellite and inter-satellite connectivity, and dense urban areas [6]. The Federal Communications Commission (FCC) and other telecom regulatories allocated sizable amount of the sub-THz spectrum as unlicensed spectrum, especially frequencies between 110 and 170 GHz. Future wireless standards that require faster data rates, reduced latency, and improved dependability to serve applications like 6G, industrial automation, and

ultra-fast wireless backhaul depend on this unlicensed sub-THz spectrum [6]. Also, because D-band signals have a small wavelength, tiny antennas can be used [17].

D-band communication is a crucial idea to investigate, but there are certain issues that must be resolved. The primary obstacles include high free-space route loss, low electronic component power efficiency, and signal propagation limitations brought on by atmospheric absorption [6]. Power generation, noise performance, and linearity at such high frequencies make it difficult to design an efficient transmitter and receiver [19]. New semiconductor technologies, including complementary metal-oxide-semiconductor (CMOS), silicon-germanium (SiGe) BiCMOS, and III-V compound semiconductors like gallium arsenide (GaAs) and indium phosphide (InP), are being investigated and developed to address these issues [4]. Greater transit frequencies (fT) and maximum oscillation frequencies (fmax) are very important for constructing effective and functional D-band circuits, so these technologies are constantly being scaled in order to reach greater values of this parameters [4]. Moreover, compact, high-performance, and scalable D-band communication systems are also being actively investigated through advancements in packaging and integration, such as heterogeneous integration and enhanced antenna technologies [17].

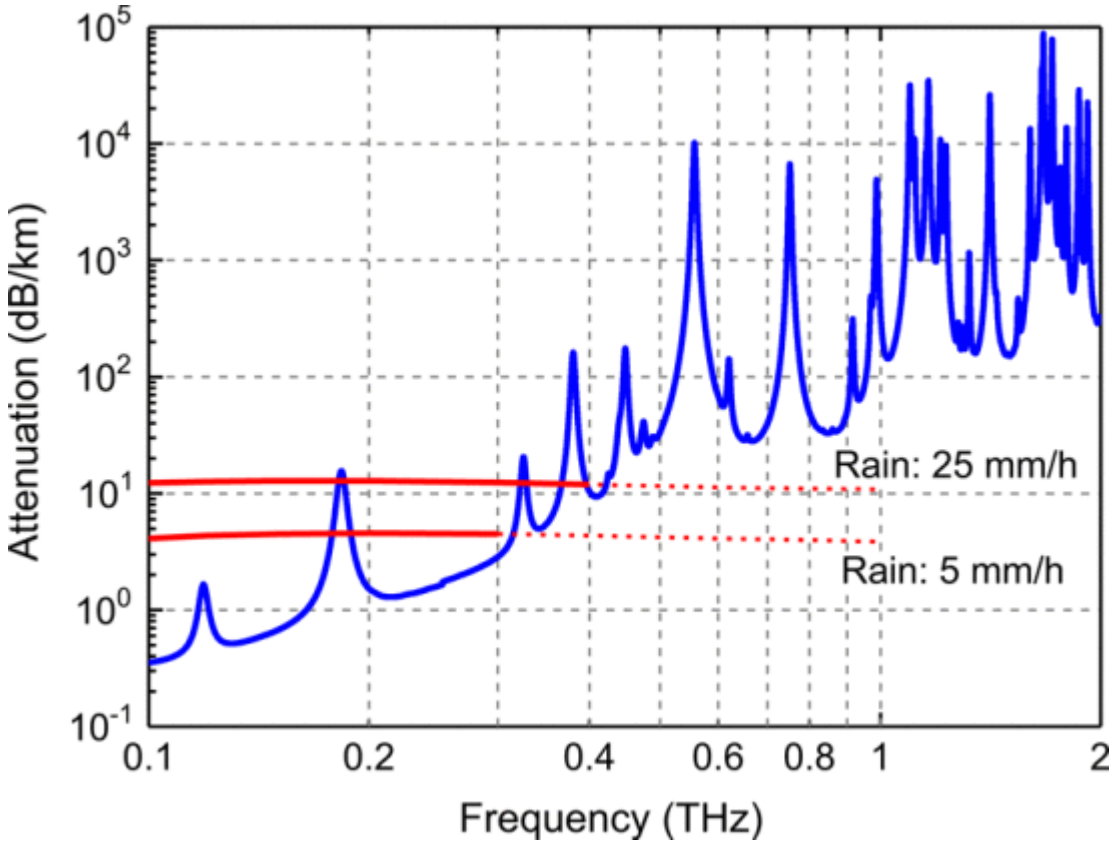

Fig. 1.2.1. Atmospheric attenuation and attenuations due to rain rates of 25 and 5 mm/h [23]

1.3. Semiconductor technology comparison for D-band frontend

In order to choose suitable technology for particular application it is needed consider trade-offs between output power, cost, noise performance, efficiency, and integration.

Starting with Indium Phosphide (InP) technology now the best technology based on its properties. As electrons move fast, the transistor's switch on and off time also very fast. [25] states that InP exhibits a peak electron velocity of approximately 2.5×10^7 cm/s. Moreover, they can handle high maximum oscillation frequency (fmax), as over 1 THz. Power Added Efficiency (PAE) also very high in this technology, as it achieved 32 % efficiency and it is essential aspect in wireless technologies. [24] Recently, 27.2 dBm output power with 14.9% PAE at 150 GHz achieved in 250-nm InP technology power amplifier. [26]

Gallium Nitride (GaN) doing well in 5G technology (28–39 GHz). It has some advantages over other technologies. One of them, it offers wide bandgap, which means material is resilient to high voltage and temperature. [27] As a GaN performance, it delivers approximately 30 dBm output power, but efficiency lower than InP. As their performance drops above 100 GHz, because they have lower fmax value.

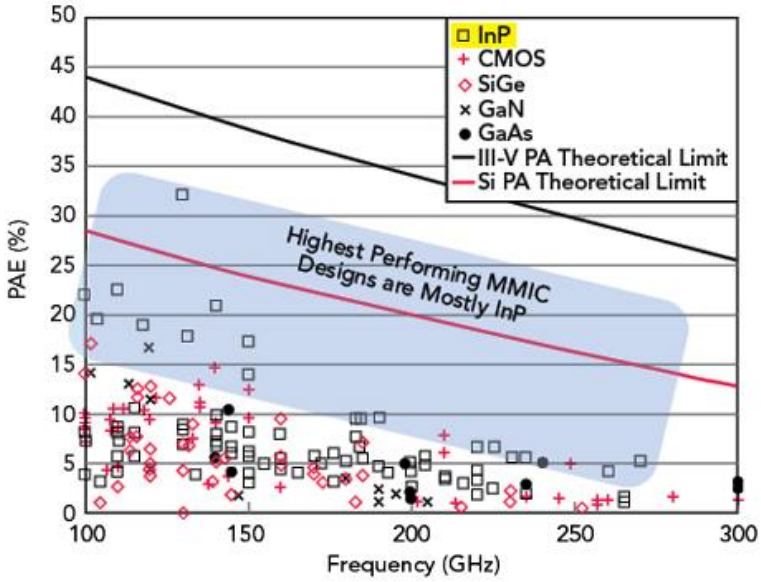

Fig. 1.3.1. Reported PA PAE results for semiconductor technologies [25]

SiGe BiCMOS and CMOS technologies combines two types of high frequency transistors (Ft and Fmax go beyond 200GHz) with CMOS for digital processing and they are good choice in designing transceivers. [29] It shows medium range of gain (15-18 dB) and suitable noise value but generally lower parameters compared with III-V compounds [30] However, theoretical study reveals that InP can achieve 45% PAE for a fixed 20 dBm output power target at 140 GHz, but SiGe are

limited to ~34% and CMOS FETs to ~32%. [28] Also, D-band operation with 9.7 dBm saturation output power at 142 GHz and 11.4 dB noise figure has been demonstrated by advanced CMOS nodes, especially 22-nm fully depleted silicon-on-insulator (FD-SOI). [31] CMOS offers high integration and less cost than other technologies which is more suitable for mass production. In the other hand, InP is more suitable for use in user equipment devices, hence, it shows optimal energy efficiency with lower number of antennas. This is huge deal because in smartphones space very limited, so it is needed have few antennas with higher efficiency. [27]

The power efficiency, signal fidelity, and possible data rates of D-band radar and communication systems are determined by the combination of these metrics: PAE, linearity, and LO phase-noise. Therefore, to meet requirement, engineers need to accurately approach to these parameters. [4]

In conclusion, optimal technology choice depends on specific applications. For long distance and high power transmission InP technology is suitable, while SiGe/CMOS is more suitable for high integration and cost effective applications like short-range communication.

Technology	**f_{max} (GHz)**	**Output power (dBm)**	**PAE (%)**	**Integration**	**Cost**
InP HBT [26]	>1000	15-27	15-32	Low	High
GaN HEMT [27]	~ 450	~ 30 (below 100 GHz)	7-34	Low	High
SiGe HBT [28]	200-500	~ 6	~ 24	High	Medium
CMOS (22 nm FD-SOI) [31]	~ 300	~ 10	~ 23	Very High	Low

Table. 1.3. Comparison between applications of technologies

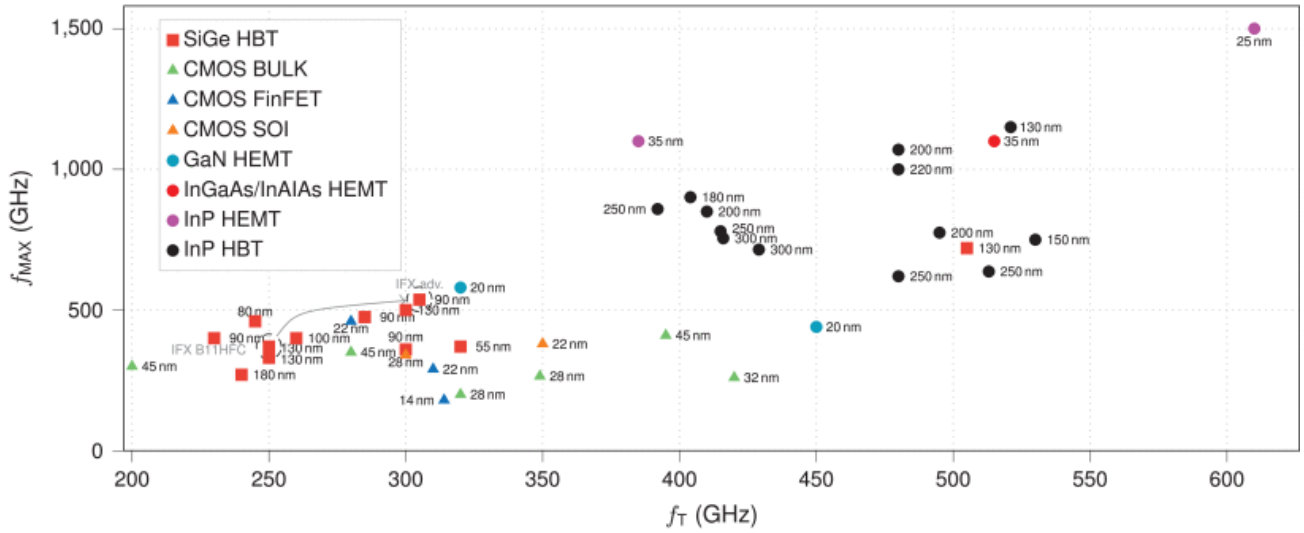

Fig.1.3.2. Semiconductor technologies for RF/mm-wave applications showing the maximum oscillation frequency versus transit frequency [6]

1.4. Overview of transmitter frontend architecture

In the D-band (110–170 GHz) or sub-THz range, the fundamental elements of a transmitter (TX) frontend typically include signal creation, amplification and power supply, modulation, and interface structures. [5] These components in literature review are often found: Signal generation or Local Oscillator (LO) sources, power amplifiers, antenna systems, modulators, buffer stages and filtering. Firstly, start with signal generators and local oscillators, because the high-frequency carrier signal is produced by these structures. This sometimes entails upconverting a signal from a lower-frequency, more stable source, such as a VCO or PLL, employing frequency multipliers, such as frequency doublers or triplers. [6][7] Phase noise affects signal quality, hence the LO signal source needs to be spectrally clean. [5]

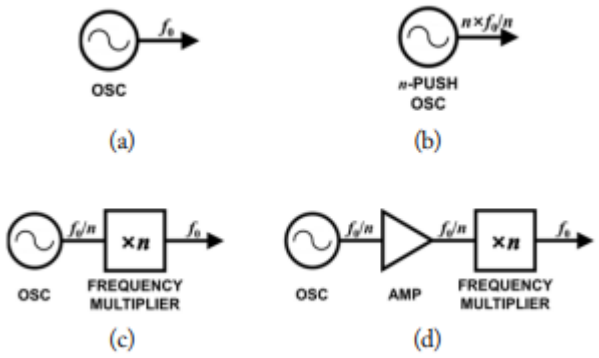

Fig. 1.4.1. Block diagrams of various topologies for signal sources to generate f_0 [7]

This scheme has been taken from [7] to explain differences and challenges of high frequency, especially D-band signal source, also analyze applied solutions. In the paper noted that it is very difficult to build directly fundamental mode oscillator (generator which works in high frequency) due to transistor limitations (f_{max}). Therefore, author proposed various alternatives:

Fig 1.4.1(a) is a fundamental mode oscillator and it is the simplest method. But it very hard for transistor to work when it gets closer to f_{max} limit. For instance, if this limit is 139 GHz, it is very hard to get stable signal after 100 GHz. [7]

Fig 1.4.1(b) represents n-push oscillator and it increases the frequency by generating harmonic signals internally. Although its efficiency can be very low.

Fig 1.4.1(c) illustrates integration with frequency multiplier. There generator works very at low frequency and frequency multiplier is added to its output. The output power and efficiency (DC-to-RF) of this method are better than the n-push method. [7]

Fig 1.4.1(d) is model with amplifier. For a frequency multiplier to work well, the signal entering it must be strong. Therefore, an amplifier is placed between the generator and the multiplier. And at [7] this method has been used.

Other part is buffer stage. We use this because we can not connect VCO directly to the power amplifier. In this case there are problems, like pulling which means powerful output signal can kick back and change frequency and the large capacitance of the PA narrows the tuning range of the VCO. [18]

Power amplifiers are needed to make signals stronger, because signals weaken over distance. [5] However, the limits of semiconductor devices make it very challenging to achieve high output power and high power insertion efficiency at D-band frequencies. The highest output power is limited by the low operating and breakdown voltages caused by the short gate lengths of transistors needed for high-frequency operation. Designers use strategies like "power combining," which combines the outputs of several amplifier stages to boost the overall output power, to get around this issue. [22]

Antennas are devices that transform energy from one state to another. It converts electrical signals inside the chip into electromagnetic waves that propagate in free space, and at receiver side it functions vice versa. In order to know how antenna works we need three main metrics: radiation efficiency, directivity gain, and beamwidth. [17]

THz antennas can be microscopically small, but this smallness leads to signal loss. To avoid this, engineers prefer directional antennas that focus the signal to a precise point, like a laser, rather than spreading it out. [17]

Antenna arrays are used to compensate for the weakness and high propagation losses of a single antenna at terahertz frequencies. These arrays combine multiple microscopic antennas in a dense area, allowing each element's phase and amplitude to be individually controlled. This allows the signal to be directed in any direction in a programmed manner (beamforming) without requiring physical movement. In order to support multiple input-output (MIMO) communications, this technology is simultaneously integrated with advanced phase shifters and front-end circuits. This maximizes the efficiency and range of terahertz communications by simultaneously managing multiple high-speed data streams and focusing signal power like a laser. [17]

1.5. Balun Design for D-Band Communication Frontends

Balun is one of the important components in the D-band frontend. It stands for balanced-unbalanced and enables the conversion between single-ended and differential signal paths. As frequency increases working with traditional transformers becomes very challenging. Because magnetic leakage happens and as wires are close to each other they stating behave like tiny capacitors, consequently it effects performance badly. Active baluns can also be used, but they have some drawbacks like higher noise and DC power consumption. Therefore, passive baluns considered best for high frequency frontends, especially Marchand baluns due to their its easy design, broad working spectrum, and capacity to support broadband balanced circuits. [32] [33]

The primary obstacle in mmWave design is not only bandwidth but also the deterioration of balance brought on by interconnects and parasitics. According to a Marchand study, electrical length directly affects amplitude and phase performance, and the transmission line that connects the two linked parts becomes a significant source of imbalance at higher frequencies. That study found that the linking connection must be electrically extremely short in order to maintain amplitude imbalance below 1 dB, demonstrating how architecture constraints start to take center stage at mmWave frequency. [32] Advanced designs include "compensated" architectures with open-circuited stubs or multiconductor linked lines to address this. By focusing on "coupling engineering" instead of just wire-length scaling, these methods produce circuits that are both more compact and able to handle a greater range of frequencies with low signal error. [34][35]

The literature shifts toward highly optimised passive design that regulate metal resistance, substrate loss, and electromagnetic leakage at even higher frequencies, particularly above 100 GHz. According to a CMOS study on a self-mixing tripler, passive devices have significant transmission

loss in the THz range. To achieve 109 GHz of 1 dB bandwidth with roughly 1 dB minimum insertion loss, a half-shielded Marchand balun was utilised. This type of half-shielded coupling structure improves design flexibility and coupling coefficient, which is advantageous when operating over 200 GHz, according to the same article. [36] Marchand baluns were employed directly in wideband matching networks in a 95 to 160 GHz SiGe power amplifier, confirming their usefulness as D-band front end building blocks despite the fact that passive loss and parasitics deteriorate with increasing frequency. [37]

Overall, conventional or transformer-based baluns can still be useful at lower microwave bands, but as operation moves into mmWave and sub-THz ranges, Marchand-based, multiconductor, compensated, and half-shielded implementations become more popular. These implementations trade geometric complexity for better bandwidth, reduced imbalance, and enhanced electromagnetic control. Lastly, maintaining balance and minimal loss while reducing area and maintaining the design's resilience to the severe parasite effects that occur frequently is the primary unresolved difficulty.

1.6. Amplifiers for communication frontends in D-band.

In the system, mostly it is needed to increase power, current or voltage of signal and it is job of amplifiers. Amplifiers have mainly 2 roles in frontend designs: Low-noise Amplifiers (LNAs) are utilized in receivers to take weak signals and power up for next steps; Power Amplifiers (PAs) boost signals to make them travel longer distances. To evaluate its performance metrics like efficiency, linearity, noise figure, stability, gain, and bandwidth are used. [38] For the high frequencies like D-band, due to parasitic effects and need to designing complex impedance matching circuits designing these elements becomes challenging. [39] Like other elements, it is difficult to design amplifiers in mmWave and higher technologies, because according to fmax and ft values. For real applications, you should build these elements far away from these values. [38] As a reference it can be checked graph in A.Alizadeh et al. work about amplifier in 250-nm InP HBT. [26]

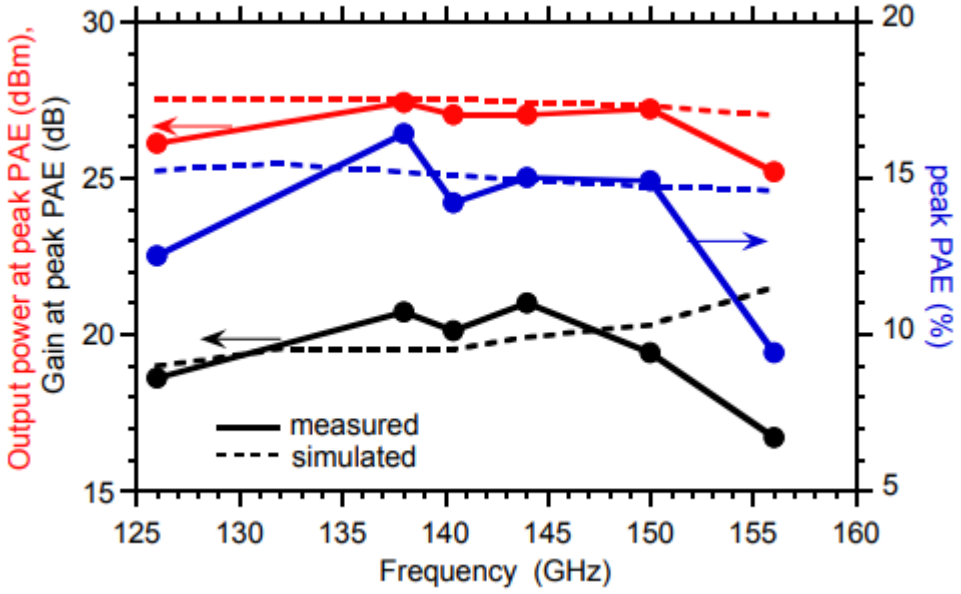

Fig. 1.6.1. Maximum PAE, with gain versus frequency [26]

The performance of high-frequency amplifiers is largely dependent on the design of impedance matching networks. Conjugate matching at the input and output ports simultaneously maximizes transducer gain for unconditionally stable devices. The matching networks must retain stability at all frequencies while converting the transistor's impedance to the system characteristic impedance, which is usually 50 Ω. A graphical method for choosing suitable source (Γ_S) and load (Γ_L) reflection coefficients that balance gain against stability margins is provided by Smith chart-based design procedures employing constant gain circles. [40]

Matching network losses become a crucial element that directly affects power-added efficiency (PAE) at D-band frequencies. Loss from matching networks or stabilization networks can drastically lower PAE above 100 GHz, requiring the creation of low-loss matching topologies. Transmission-line-based (LB) networks and stacked transformer-based (TB) matching networks are the two main implementation strategies that have been studied. While transmission-line-based networks can achieve greater quality factors and lower loss at the expense of wider area, transformer-based matching offers compact dimensions and broadband characteristics. [24] [41]

1.7. Passive elements at D-band communication frontends.

Passive components like capacitors and inductors no longer function as perfect, predictable parts at 110–170 GHz frequencies. The tiny wavelength of the signal causes parasitic effects, like energy seeping into the chip substrate and electricity packing the surface of wires and this is called

as the skin effect occurs. The components' efficiency also known as Q-factor is decreased as a result of this degradation. In order to account for these inevitable physical losses, modern 6G design necessitates a design with active element together approach in which active transistors and passive interconnects are modelled and optimized together. As frequencies enter the D-band, on-chip inductor efficiency, as determined by the Quality Factor (Q), drastically declines. Metal resistance, energy leakage into the silicon substrate (eddy currents), and current crowding effects such as skin and proximity effects all contribute to this decrease. Designers who make these components need to employ thicker metal layers and specialized shielding to retain performance. Even with these improvements, D-band inductors usually only reach Q values of 10–20, which is a considerable decrease from the 30–50 range observed at lower frequencies. [42] The study emphasizes the constraints of nesting inductors within one another at sub-THz frequencies, despite the fact that this technique is frequently used to save valuable chip area. The closeness of these windings causes a change in the distribution of current in the 22 nm FD-SOI process as noted by authors of [43]. Although this interference is insignificant at lower frequencies, it becomes destructive over 100 GHz, resulting in unpredictable losses that can seriously impair the Low-Noise Amplifier's (LNA) performance.

Although Metal-Insulator-Metal (MIM) capacitors have long been a mainstay of RF design, excessive parasitic resistance and via losses cause their performance to drastically deteriorate in the D-band. According to recent research, Metal-Oxide-Metal (MOM) capacitors attain a Q of 400 at 60 GHz, while MIM capacitors only display a Q of 25. MOM structures offer a more reliable, economical, and effective solution for the interstage matching networks needed in sub-THz power amplifiers by utilizing the thick top-metal layers of the CMOS or SiGe process. [44] In the work done by Chang_Shu et al. [37] to lower passive losses in matching networks authors changed MIMI capacitors with Metal-Oxide-Metal capacitors.

In the transitional regime of D-band filters, neither fully distributed nor completely lumped models are adequate. Recent research investigates hybrid "quasi-lumped" topologies that combine microstrip inductors and interdigital capacitors in order to overcome this. These designs provide low insertion loss (<3.5dB) and sharp stopband rejection in a small footprint by introducing transmission zeros through mutual coupling. This hybrid approach successfully strikes a balance between the limitations of on-chip area and the requirement for electromagnetic precision. [45]

To summarize, literature review about passive elements design in high frequency systems shows that distinction between "device" and "parasitic" practically disappears. So, every inductor is also a capacitor to substrate, and also every capacitor is a series RL network, every balun could be an asymmetric delay line, and every filter response is also a statistical distribution. Therefore, the

methods and concepts that have been analyzed are done to successfully overcome these issues in D-band frequencies.

1.8. CMOS Transistor-Based Frequency Multipliers

Diode based multipliers also used in such systems and most popular device is Schottky diode. But it is challenging to integrate them with amplifiers and oscillators. Also, they have low efficiency, it means that if input signal is low, at the output signal power is low, so it is low gain. In diode-based multiplier isolation between input and output considered another challenge. [10]

However, even at low input power levels, transistor-based multipliers can raise the conversion gain by utilizing the transconductance of the transistor to increase the voltage swing at input and output nodes. And isolation in these devices is not problem, as two-port devices can be used. Transistor-based multipliers have advantage which is valuable in CMOS technology chip fabrication that they are easily integrated with other blocks. [10]

Some papers have been analyzed and main parameters and key takings have been noted in there:

- A $220\,\text{GHz} \times 2$ amplifier–doubler chain fabricated in 40-nm bulk CMOS has been analyzed by author in [11]. In this work, this device is achieving a peak output of 7.9 dBm at 200 GHz with a 30 GHz 3 dB bandwidth. To suppress parasitics in this work balun has been deployed. [11]
- According to [12], 45-nm CMOS SOI doubler and 40-nm CMOS self-mixing tripler have been analyzed and compared. First is a balanced doubler operating from 135 to 160 GHz in 45-nm CMOS SOI delivers +3.5 dBm peak output (-4.5 dB conversion gain) when driven by 7 dBm input at 70-80 GHz. And second is a self-mixing tripler in 40-nm CMOS covers 195–244 GHz and parametrics are 49-GHz 3-dB bandwidth. [12]
- 65nm CMOS 60GHz PA/Mixer: While not a multiplier, a 60GHz transmitter front-end in 65nm bulk CMOS exhibits a PA with 8.5% PAE and 9dBm saturated output, offering helpful building blocks for lower-band multipliers. [13]

Modern 40–65 nm CMOS processes may produce usable power levels (~ +3–8 dBm) at low THz frequencies utilising optimised balanced topologies, as shown in [11], [12], and [13].

1.9. Impedance Matching and Harmonic Selection Networks

A frequency multiplier works in principle that taking sine wave and distorting it. This distortion multiples original frequencies and creates harmonics. It is known that typically source impedance is 50 Ω, the input-matching network of a CMOS frequency multiplier converts to the ideal complex impedance that the transistor perceives at the fundamental frequency (f_{in}). By doing this, the large-signal drain current swing that produces the nonlinear waveform is maximized. At the output of transistor there are some frequencies like f, 2f, 3f, and so on. But one of them is needed, in that case output matching circuit behaves like filter. It passes needed frequency, blocks other ones. As shown in a V-band CMOS tripler [15], where the interstage network simultaneously matches the third-harmonic impedance and rejects the fundamental and even harmonics without adding loss, a balun provides differential drive and common-mode suppression for odd-order multipliers. Varactor-tuned impedance-matching filters are used when tunable or wideband performance is needed. According to [15], it is possible to achieve minimal insertion loss (≈1.5 dB) and a wide impedance span by tuning a second-order Chebyshev filter loaded with varactors to maintain the necessary complex impedance over a wide range of source and load fluctuations.

1.10. Harmonic Generation Mechanism in CMOS Transistors

In order to generate harmonics in CMOS transistors for frequency multiplication, the device must be driven into a highly non-linear state. Class-C operation, in which the transistor is biassed well below its threshold voltage (V_{th}) is usually used to accomplish this. When a strong input signal is applied, the transistor's behavior changes; otherwise, it stays off state by default. The transistor acts as a non-linear switching element when an input RF signal is superimposed onto this low DC bias point. [16] The transistor only conducts current during the few intervals when the RF signal peaks push the gate voltage above V_{th} since the gate voltage V_g is maintained below the threshold. Instead of a continuous wave, this produces a pulsed drain current I_{DS}. This pulsed waveform has several higher-order frequencies in addition to the original frequency, making it mathematically rich in harmonics. [16]

A Taylor series expansion of the drain current around the DC bias point can be used to analyze this process mathematically.

$$I_{DS} = I_0 + a_1 v_{in} + a_2 v_{in}^2 + a_3 v_{in}^3 + \cdots \quad (1.10.1) \text{ [5]}$$

- $a_1 v_{in}$ – input signal
- $a_2 v_{in}^2$ – produce the second harmonic 2(f_{in})

- $a_3 v_{in}^3$ – produce the third harmonic 3(f_{in})

Designers can optimize the power of the intended harmonic by purposefully raising these non-linear coefficients through particular biasing. [5][16] By decreasing the DC gate bias voltage V_G the pulse duration of the drain current becomes shorter. This action strengthens the harmonic content of the output current relative to the fundamental tone. For instance, reducing the bias deepens the distortion in the waveform, improving the third harmonic relative to the fundamental, which is essential for efficient tripling. [16]

For doubler when transistor works in Class-C regime second harmonic is strong. However, to raise the third harmonic, clipping alone is insufficient. The conversion efficiency is increased by using waveform shaping techniques. [16]

1.11. Output Power Limitations and Optimization in CMOS Multipliers

In CMOS frequency multipliers working at D-band and THz frequencies, achieving high output power (P_{out}) is severely constrained by the semiconductor devices themselves. [17] The maximum possible output power is limited by short gate lengths, which are necessary for high-frequency operation and result in lower operational and breakdown voltages. Furthermore, power amplification stages are hampered by CMOS transistors' decreasing small-signal gain when frequency approaches f_{max}. [17][20] Designers maximize the use of the transistor's nonlinear properties by optimizing performance using particular topologies. Traveling-wave multipliers, which use counter-propagating signals to create constructive standing waves at the transistor gates and improve voltage swing and harmonic power output, are a crucial optimization approach. Utilizing this technique, a frequency doubler implemented in 65 nm CMOS demonstrated a peak output power of 6.6 dBm at 244 GHz [10]

Self-mixing structures or cascading multiplier stages to improve output are other strategies for optimizing and this technique have been applied in plenty of works. For instance, one CMOS self-mixing tripler achieved a peak output power of −6.3 dBm [21], while a cascaded multiplier chain in SiGe BiCMOS reached +2.9 dBm for a tripler operating between 75–96 GHz [21].

2. Modelling of D-band frontend circuit and components.

Keysight Advanced Design System (ADS) serves as the primary tool in this work for designing, simulating RF and microwave components. Design flow firstly started as using ideal elements to build circuits for this application, simulate and measure results. The integrated 3D planar electromagnetic simulator ADS Momentum was used for passive component design in order to precisely represent on-chip balun, inductors and capacitors at these frequencies. In order to account for foundry-specific parasitics and process changes, ADS is offering a unified environment where individual components were combined for the entire frontend circuit. As example, in this work, ideal transistor was replaced by Process Design Kit (PDK) model which provided by foundry.

2.1. Block scheme of frontend system.

Block scheme (fig.2.1.1.) represent simplified version of the system, although system is more complex circuit with lots of passive and active elements. Specifically, it is needed to build matching network before steps. Each block's circuit and/or layout design will be shown in the next subparagraphs with simulation results.

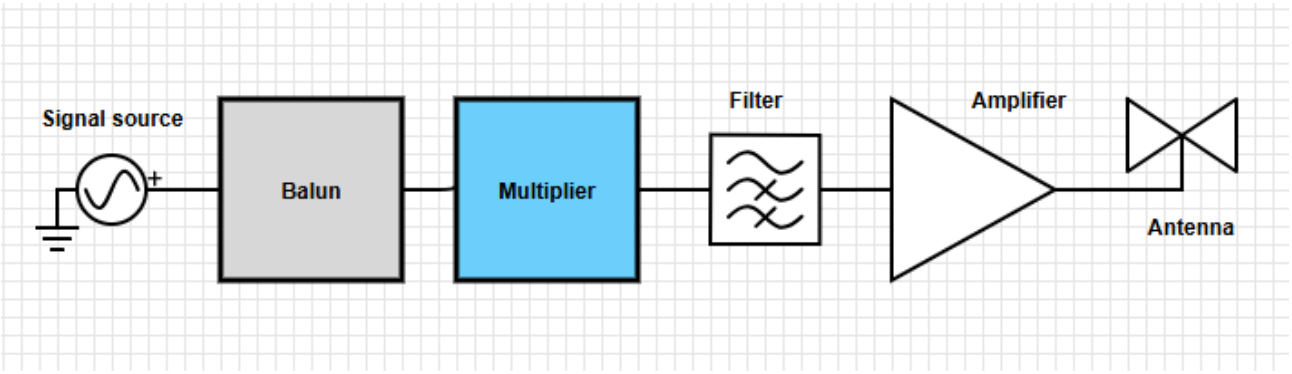

Fig. 2.1.1. Block scheme of D-band transmitter

System starts with signal generation with the output power of 10 mW. As noted in literature review, balun converts single-ended signal to differential signal which is needed for next stages. Moreover, it has benefit for even-harmonic rejection. Multiplier in this block scheme triples input frequency. It means that, this tripler generating third harmonics due to nonlinear elements. The filter part intended to guarantee efficient and loss-free passage of desired third harmonic signal, while blocking other harmonics. The next step is amplifier which boosts filtered signal and it goes to antenna to radiate. Doubling to D-band frequency also happens in this stage.

2.2. Substrate design

The simplified CMOS model has been built within ADS Momentum substrate stack model to use in EM simulations.

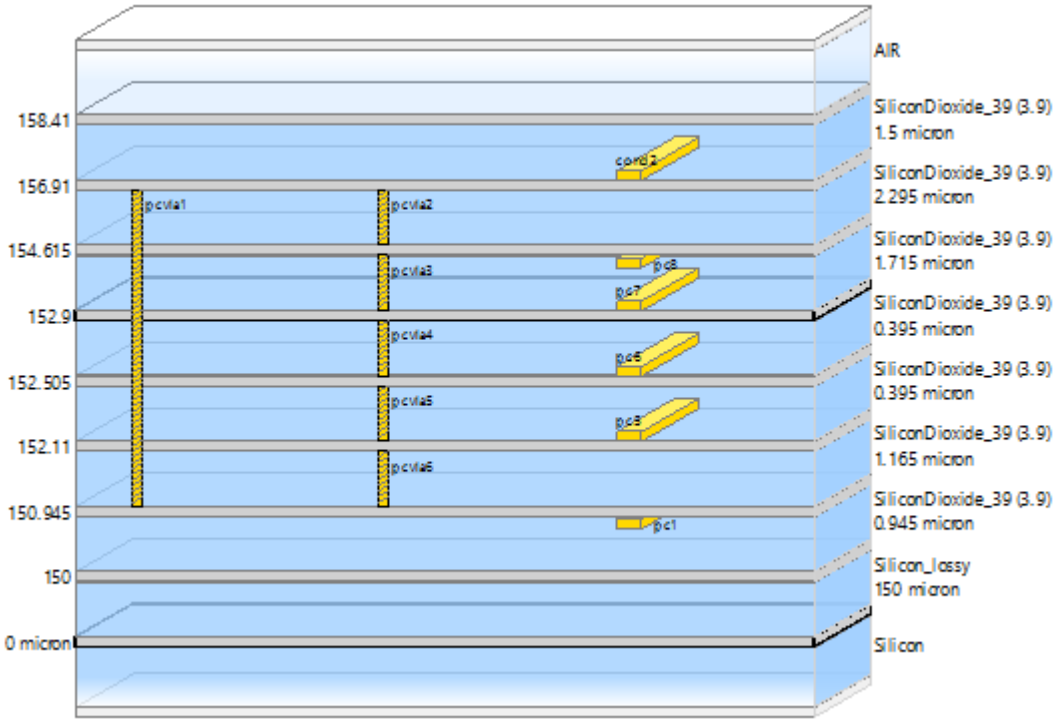

Fig 2.2.1. Simplified substrate for EM simulation

Fig 2.2.1. visualize substrate model which has been used to simulate layout design of components like capacitors, inductors and so on. It consists of 3 regions: lossy silicon bulk substrate, seven silicon dioxide dielectric layers, and multiple metal interconnect layers.

2.3. Balun

Layout of balun has been designed as shown in fig. 2.3.1. in ADS layout designer. For the tripler, the balun guarantees that the two parts of the differential pair have the proper phase relationship, which suppresses even-order harmonics and strengthens the intended third harmonic output.

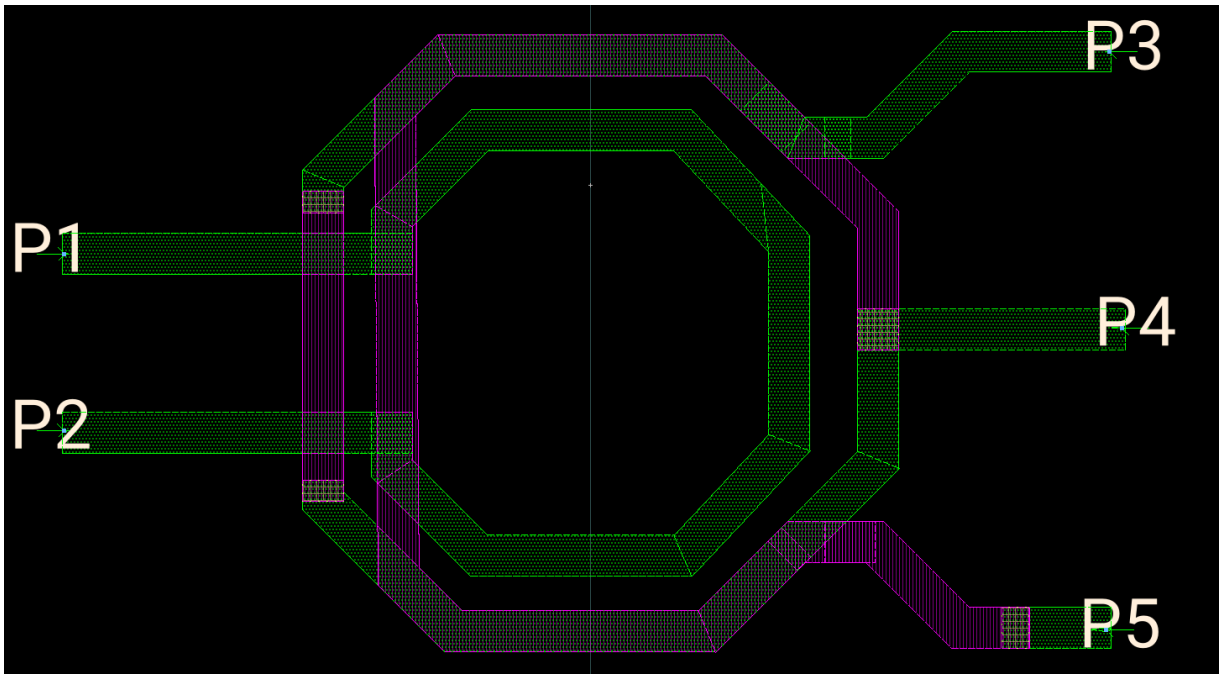

Fig. 2.3.1. Layout of balun

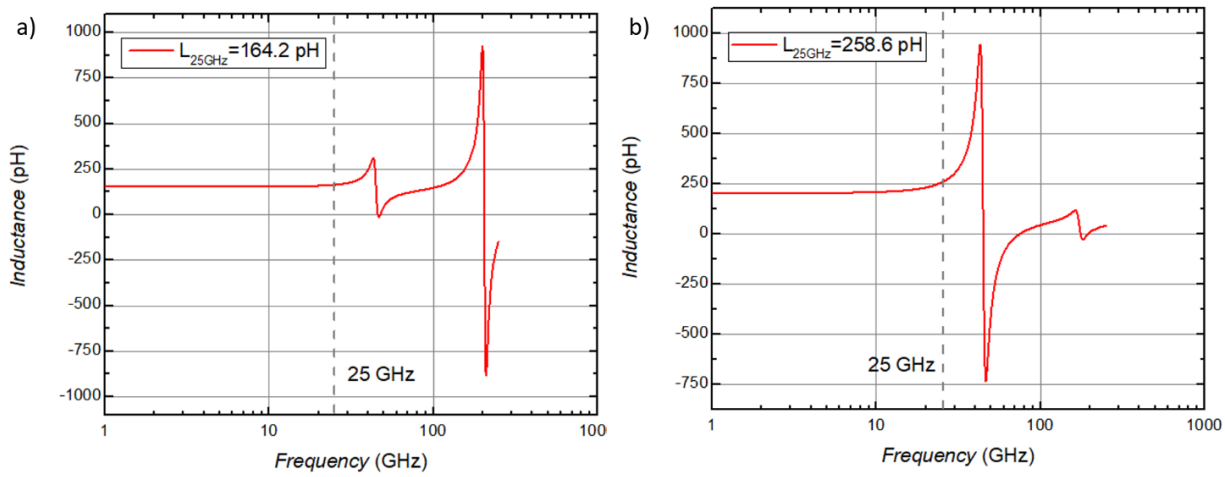

Fig. 2.3.2. Effective inductance at a) port 1 b) port 2 of balun

Fig. 2.3.2.a) shows effective inductance of balun port 1. Around 25 GHz which is the frequency interval that balun operates in this system inductance shows 164.2 pH. At 200-210 GHz graph shows resonance, it means at this range structure is stopping behave like inductor, goes to capacitive behavior. It proves that balun designed well below from resonant frequency. Fig 2.3.2.b) plotted inductance of balun port 2. In this graph resonance has been seen at 50 GHz and it shows different inductance value. First one informs about inductance character of the unbalanced winding (single-ended side), second one inductance character of the unbalanced winding (differential side). It is normal that inductance values are not same, because windings have different structures.

2.4. Tripler designs

After transformation to differential signal by the balun component next main component in tripler. Suppose the input signal is f_{in} because of nonlinearity of transistor output signals contains $2f_{in}$, $3f_{in}$, $4f_{in}$ etc. Inductors before transistors is used for input impedance matching.

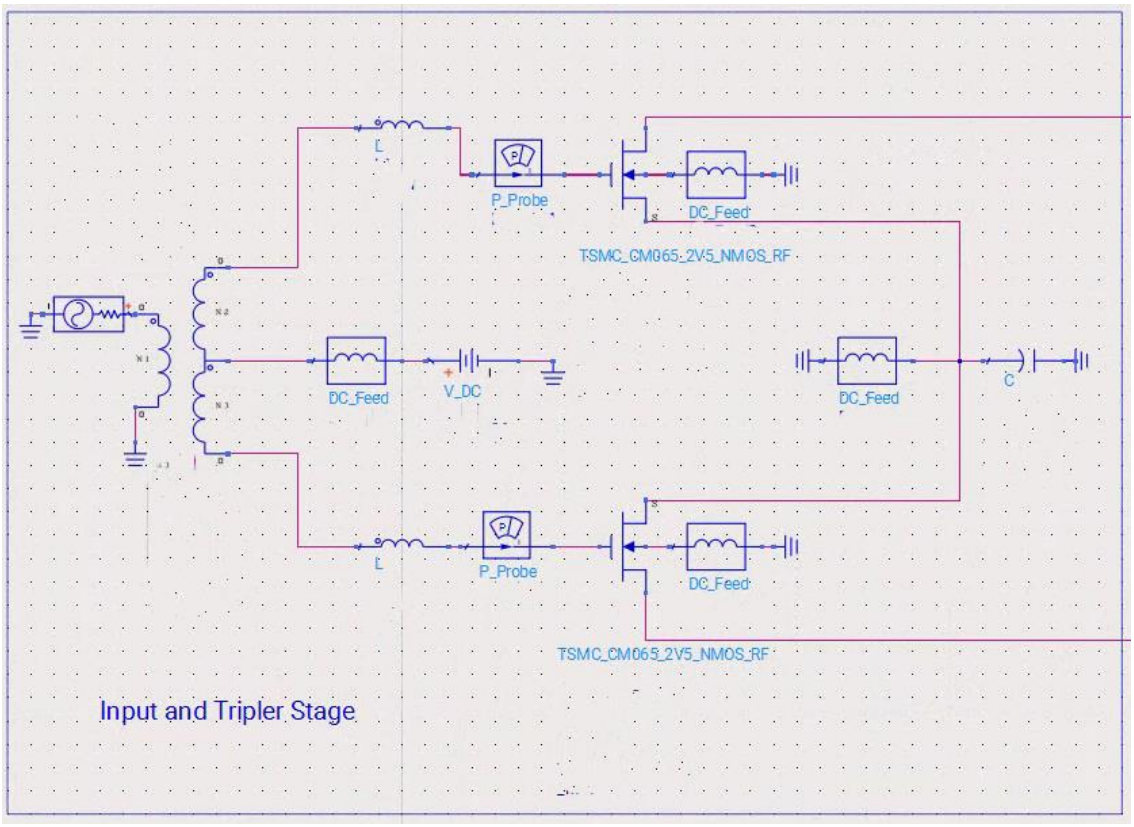

Fig. 2.4.1. Input and tripler part of circuit

Fig. 2.4.2. intended to show input and output powers after tripler.

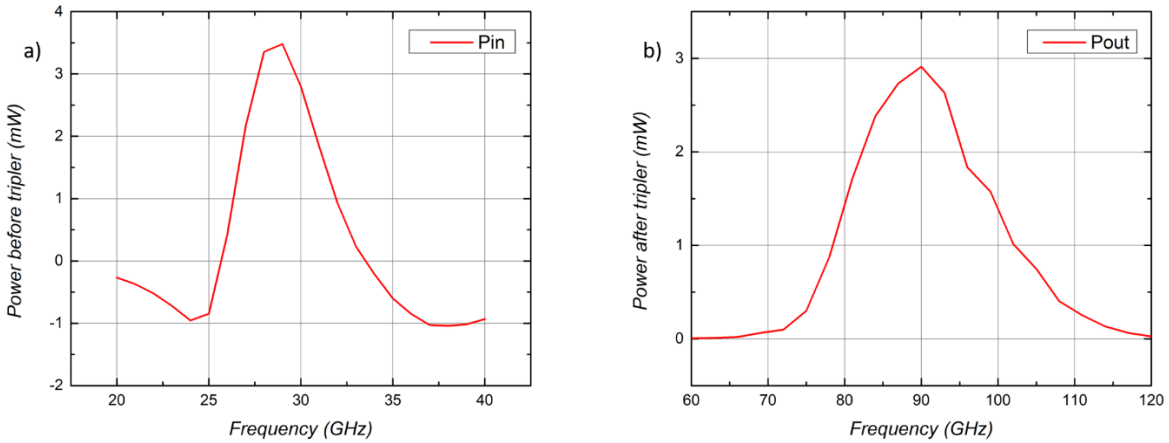

Fig. 2.4.2. a) Input and b) output power in tripler

2.5. Filter design

Then it is needed to make filter as frequency-selective network to get harmonics that needed in system. Fig 2.5.1. illustrates filter design at circuit level.

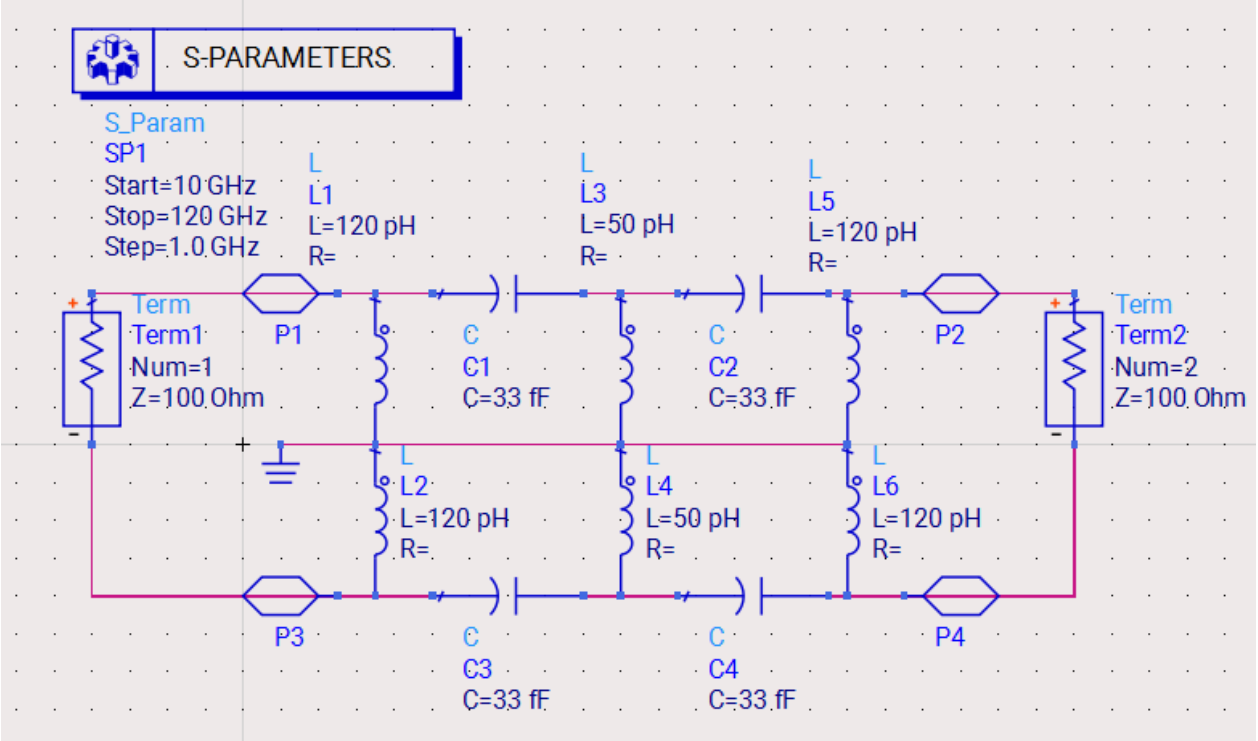

Fig. 2.5.1. Filter circuit

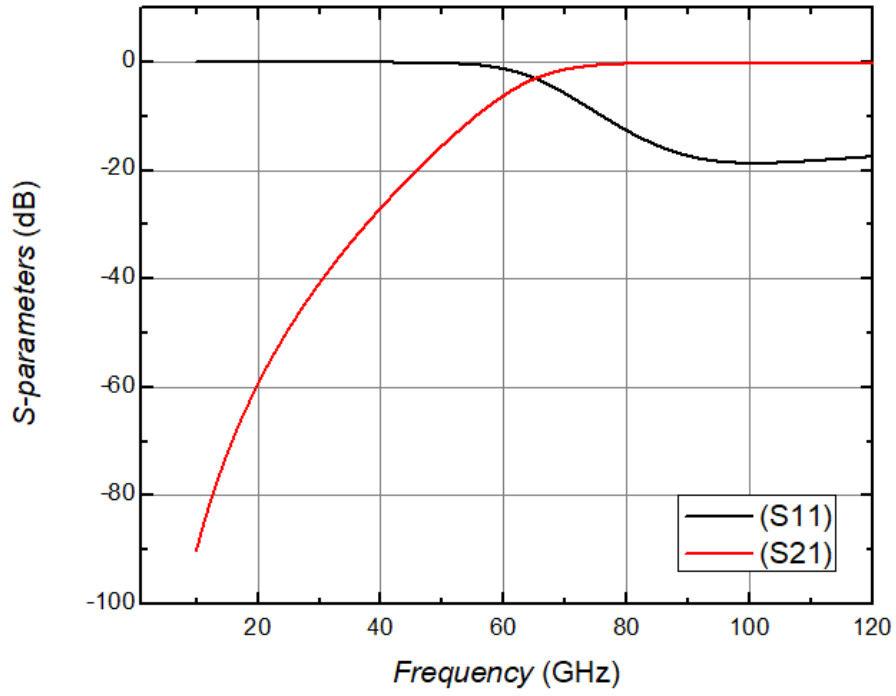

Fig. 2.5.2. S-parameters of circuit design filter

S11 and S22 represents return loss and transmission respectively. Fig 2.5.2. shows transmission happens after 65 GHz, before these frequencies it is very low which works as stopband. At this frequencies S11 is 0, it means that signal reflected.

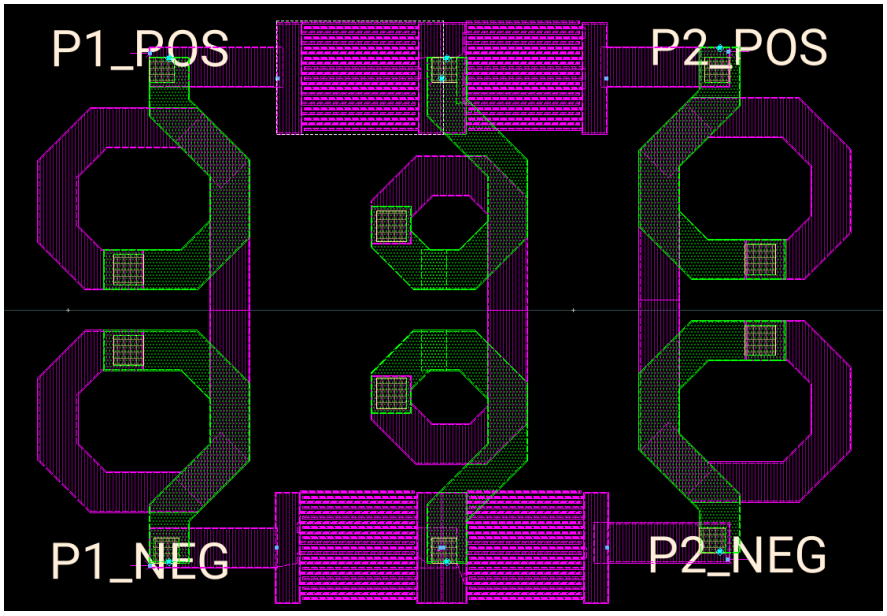

Fig. 2.5.3. Filter layout design

Based on circuit layout of filter also designed with real elements and simulated. As this filter is differential filter it has positive and negative ports, so signal is carried by two lines with opposite phases.

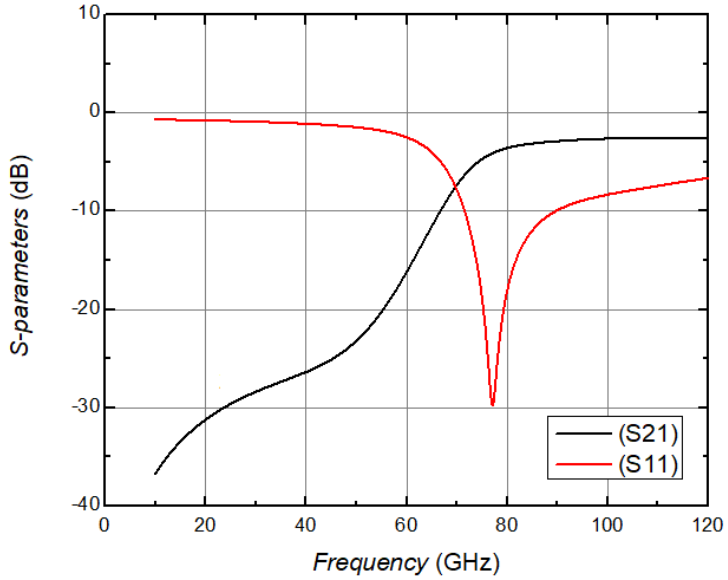

Fig. 2.5.4. Filter layout design S-parameter results

Fig. 2.5.4. depicts performance of layout design and filter works. Although it can be seen between Fig. 2.5.2. and Fig 2.5.4. performance of the layout design is different from ideal circuit. It is caused by parasitic effects and losses due to the physical implementation.

2.6. Amplifier

This designed circuit is a differential multi-stage RF amplifier. Cascaded common-source differential stages with inductive loads make up the architecture. Interstage capacitors block DC components while providing AC connectivity between stages. In the bias network, inductors serve as RF chokes as well as for load adjustment. The differential arrangement increases stability at high frequencies and strengthens resistance to common-mode noise. To guarantee effective power transfer to a 50 Ω load, output matching networks are used.

$$G = \frac{P_{out}}{P_{in}} \quad (2.6.1)$$

Formula 2.6.1 has been used to describe amplifier's gain. The Fig. 2.6.2. shows that amplifier works at targeted frequency range.

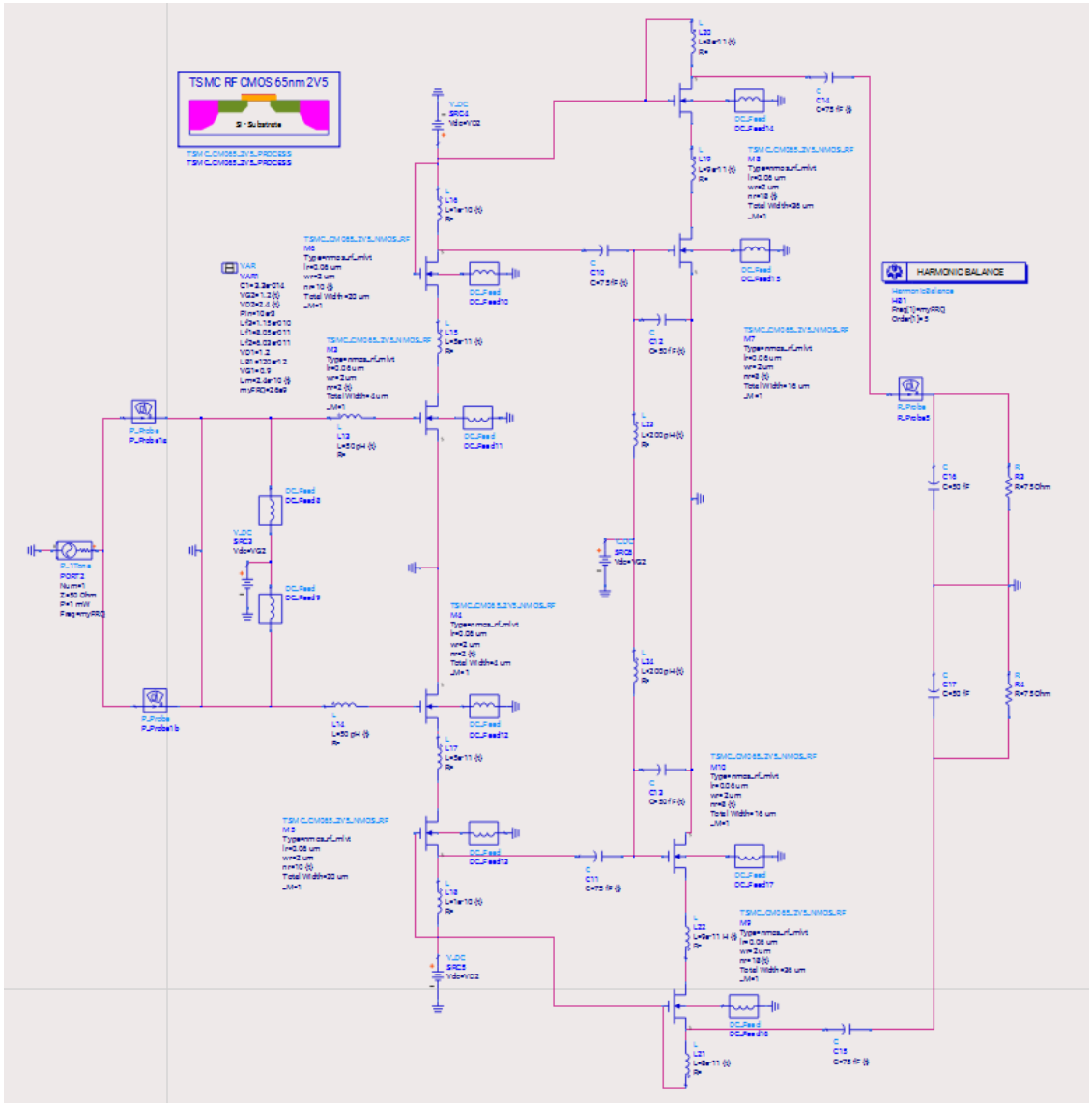

Fig. 2.6.1. Amplifier circuit

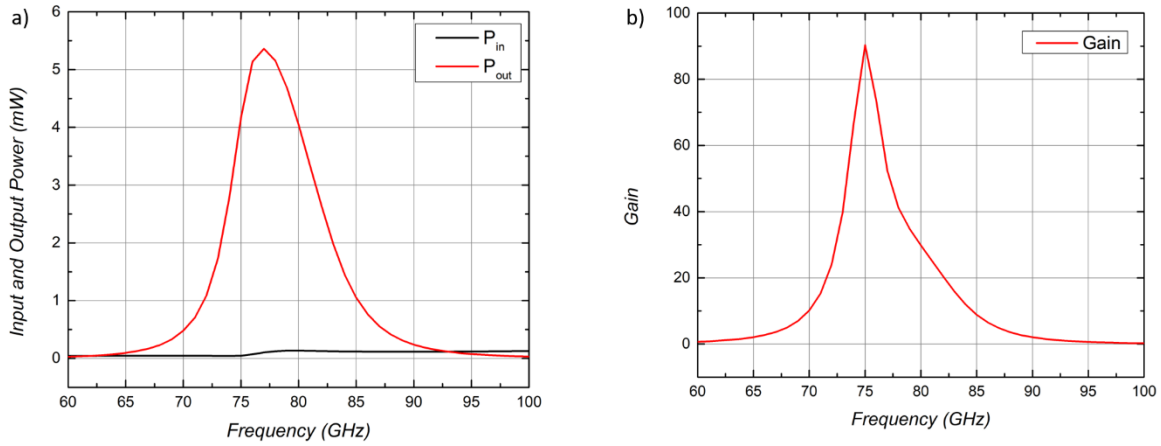

Fig. 2.6.2. a) Power in input and output of amplifier b) Gain of amplifier

2.7. Antenna

For application in D-band frontend system H-dipole antenna with bowtie modification integrated with cavity has been designed. Layout view of this antenna designed in ADS software and has shown in Fig 2.7.1:

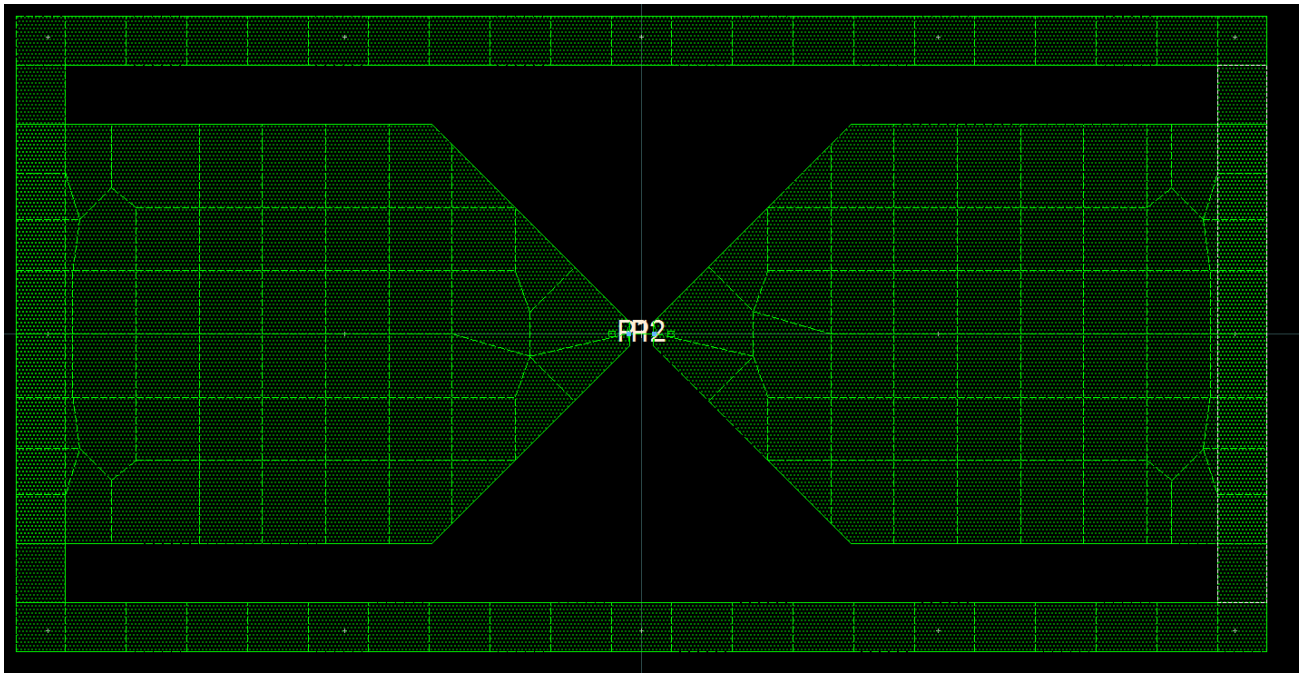

Fig 2.7.1. Antenna layout

Antenna designed as two flared wings that are triangular in shape meet at a central feed point and cavity. By making antenna in this shape, we make it to operate wider frequency range and cavity helps energy directed efficiently. Beside it, energy frequently becomes trapped in the substrate and moves sideways, resulting in interference and power waste. These waves are reflected and forced to contribute to the antenna's primary radiation beam by the cavity, which serves as a barrier.

Figure 2.7.2. illustrates return loss of antenna. S11 basically means how much power radiated back instead of radiating it. 0 dB means all power is reflected and mostly -10 dB is standard. It works at very wide band, as well as, targeted frequency range for D-band.

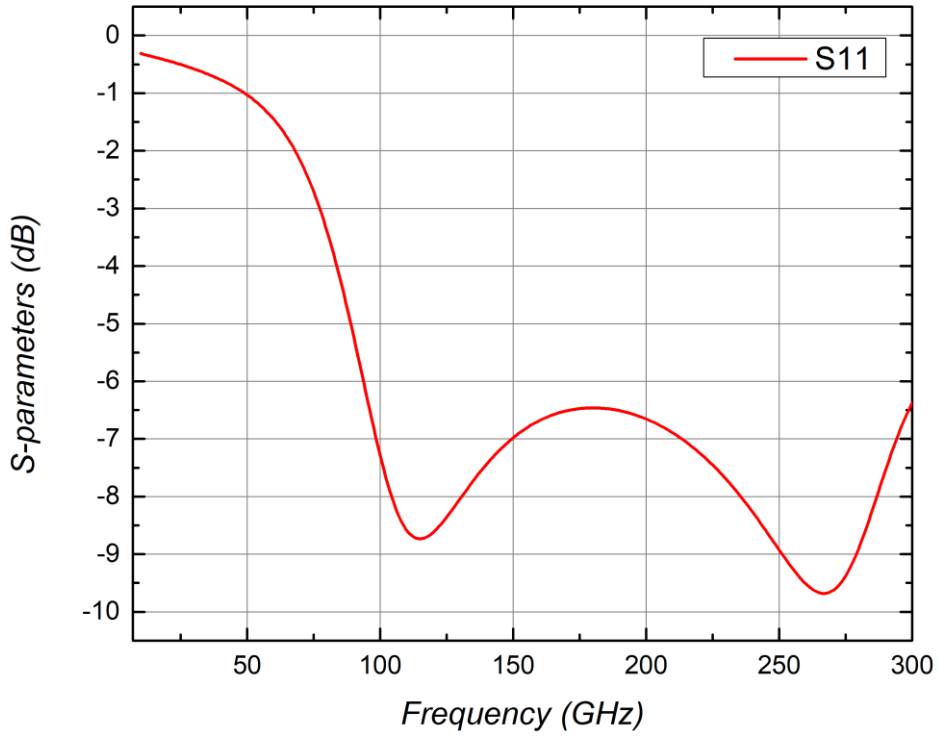

Fig. 2.7.2. S11 analysis of antenna

2.8. Passive elements modelling.

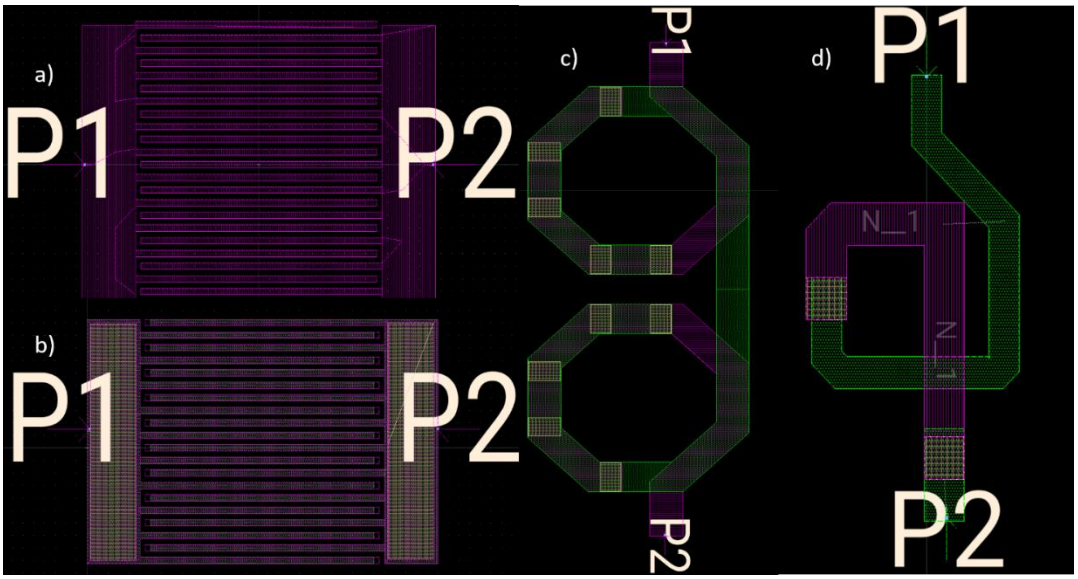

Fig. 2.8.1. Layout model of a) 28 fF b) 71 fF capacitors; c) 270 pH d) 57pH inductors

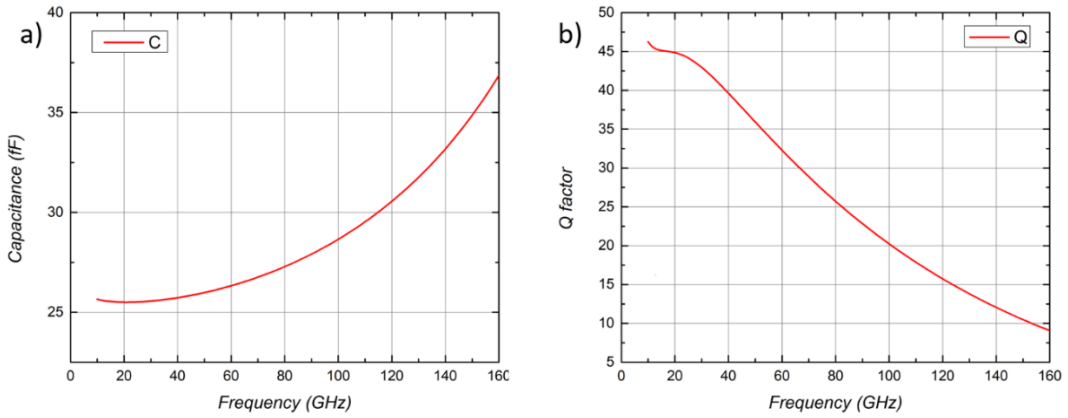

Fig. 2.8.2. a) Capacitance b) Q factor of 28 fF capacitor

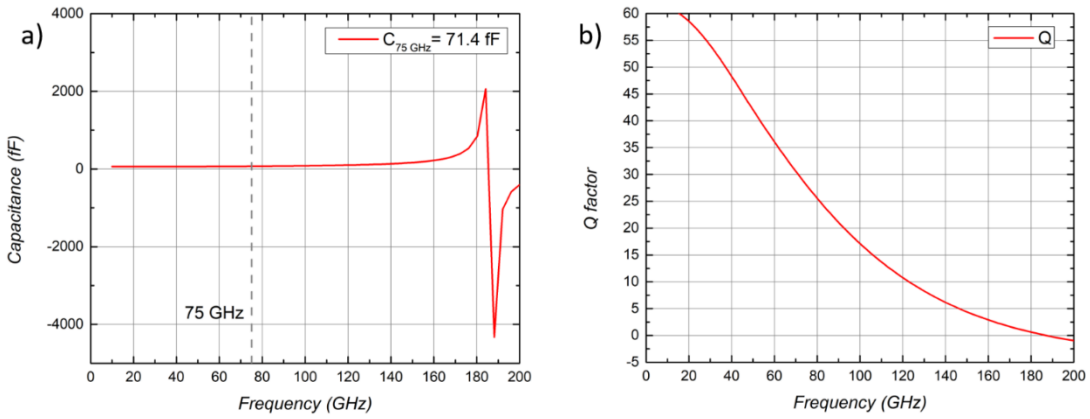

Fig. 2.8.3. a) Capacitance b) Q factor of 71 fF capacitor

Electromagnetic modelling was used to assess the developed element's electrical performance. Fig. 2.8.2. and fig. 2.8.3 shows design results of capacitors. Formula 2.8.1 has been used to obtain capacitors quality factor. Z is impedance of capacitor:

$$Q = -\frac{imag(Z)}{real(Z)} \quad (2.8.1)$$

Q factors are 26 and 30 for these capacitors and these are consistent with typical elements in CMOS technologies operating in these frequencies.

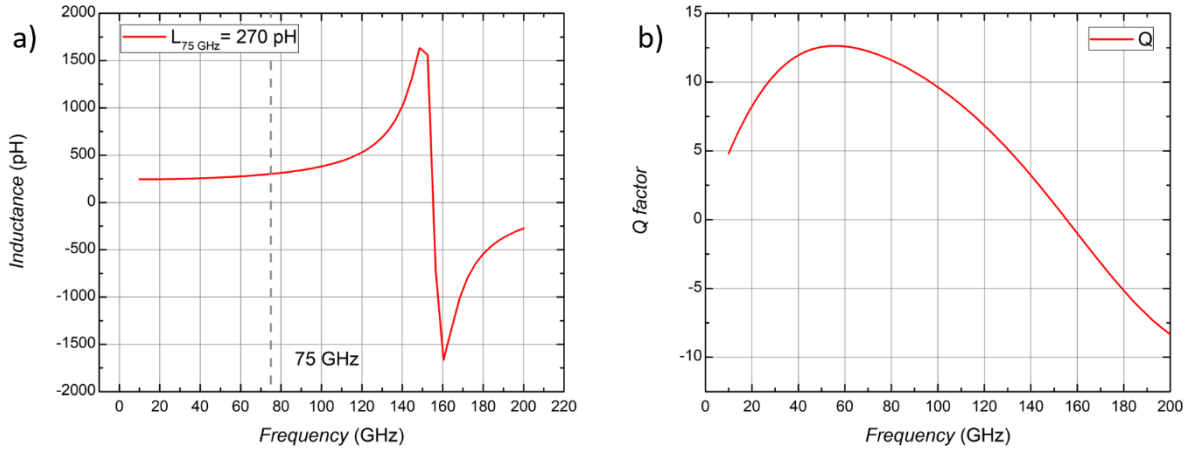

Fig. 2.8.4. a) Inductance value b) Q factor of 270 pH inductor

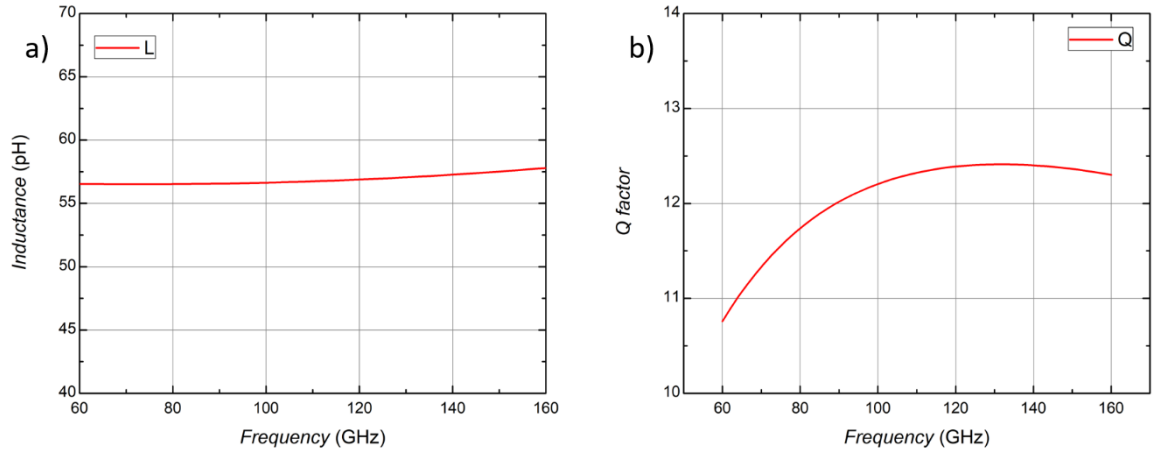

Fig. 2.8.5. a) Inductance value b) Q factor of 57 pH inductor

Same has been done for assess inductor's performance. Fig. 2.8.5. a). depicts the inductance variation as a function of frequency. The inductance, which varies from roughly 57 pH at 75 GHz, is comparatively constant. This only slight fluctuation shows that the chosen inductor has adequate frequency stability.

$$Q = \frac{imag(Z)}{real(Z)} \quad (2.8.2)$$

Formula 2.8.2 used to extract 11.5 and 12.5 Q factor values in inductors, these are also typical values for these elements.

2.9. Doubling and overall system result.

The nonlinear nature of the MOS transistors in the proposed circuit allows for frequency doubling in the amplifier's last stage. The nonlinear drain current characteristic of the gate produces harmonic components of the input signal when a large RF pulse is introduced and with the load, in this case antenna, we can see 6th harmonic which is in D-band. Consequently, the amplifier does both frequency multiplication and signal amplification at the same time.

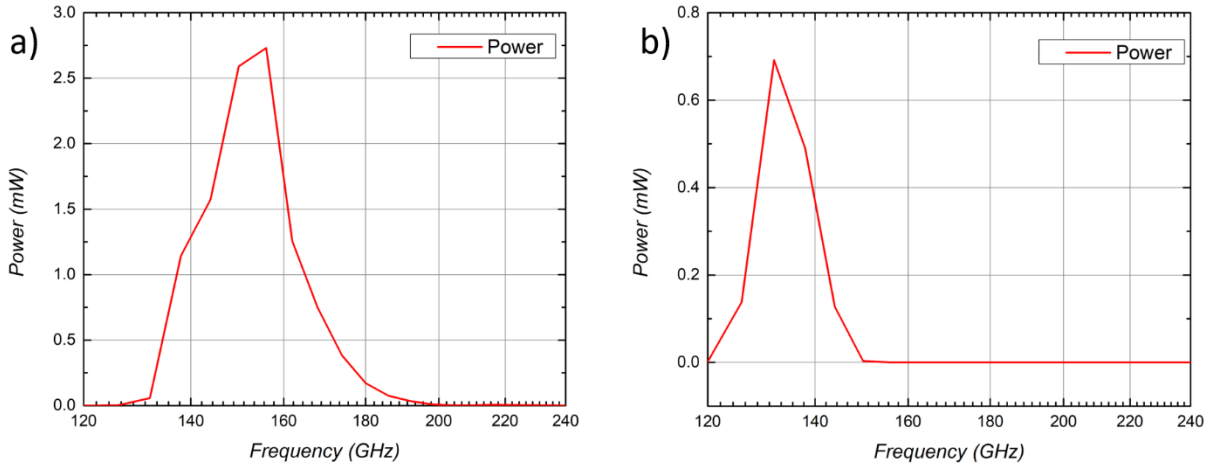

Fig. 2.9.1. Simulated output power in circuit with a) ideal and b) real elements

From the fig. 2.9.1., it is observed that, performance is different when it is used real or ideal elements in the circuit. Ideal components do not consider substrate losses, parasitic resistances, or other non-ideal effects since they assume perfect behavior. As a result, power is not dissipated and gain and output power is high. Real components, on the other hand, have a number of imperfect properties, including substrate coupling, parasitic capacitances, not ideal Q factor and so on. As a result, some of the RF power is not delivered to the load but rather wasted as heat. As it noted in literature review, especially in millimeter-wave frequencies this effects performance more prominently. Therefore, simulation with real elements is more accurate to real life performance. We got 0.7 mW with the real elements that have been designed. That is good for further process, which is radiating power by the antenna.

3. Chip implementation and Characterization.

3.1. Prototype Chip.

To validate modelled frontend architecture prototype chip in CMOS technology has been fabricated. This chip also can be considered as proof of D-band frontend design concept that implemented in this work. The chip design for D-band frontend also already submitted. Submitted design uses the same design principles, passive component structures and similar topology of circuit. Fig. 3.1.1. picture of fabricated chip has been taken in microscope and size of chip is 1×0.5 mm.

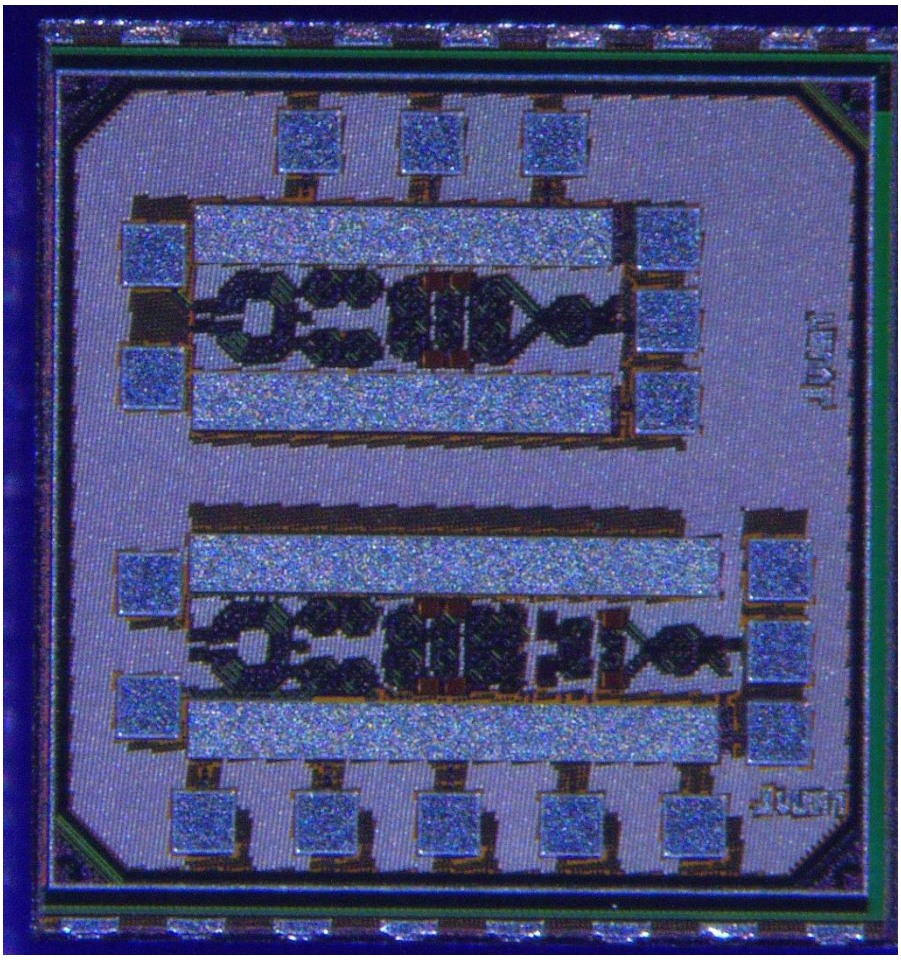

Fig. 3.1.1. Picture of produced chip

Upside of picture is only tripler and downside circuit is tripler with amplifier. Tripler multiply the frequency, while amplifier increase output power of generated signal. The large square metals in chip are pads. They are located at the edges of chips and used for RF probing during measurements, DC bias voltages and connections to ground. As modelled circuit in previous paragraph circuit starts with balun and middle part of circuit are tripler before filter. It receives differential signal, due to nonlinear transistor operation generates harmonics and subsequently matching network selects desired harmonic. In the chip that have amplifier this signal power is boosted due to next stage.

3.2. Transistor I-V characteristics.

Understanding the electrical behavior of the active components in a circuit and identifying suitable biasing conditions are made possible by analyzing the current-voltage (I-V) characteristics of transistors. The link between the drain current I_D, the drain-source voltage V_{DS} and the gate-source voltage V_{GS} is shown by the I-V characteristics. The various operational regions of the transistor, such as the linear region and the saturation region, can be identified by examining these features. An essential MOSFET parameter that describes the connection between the input gate voltage and the resultant drain current is the transconductance, or g_m.

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \quad (3.2.1)$$

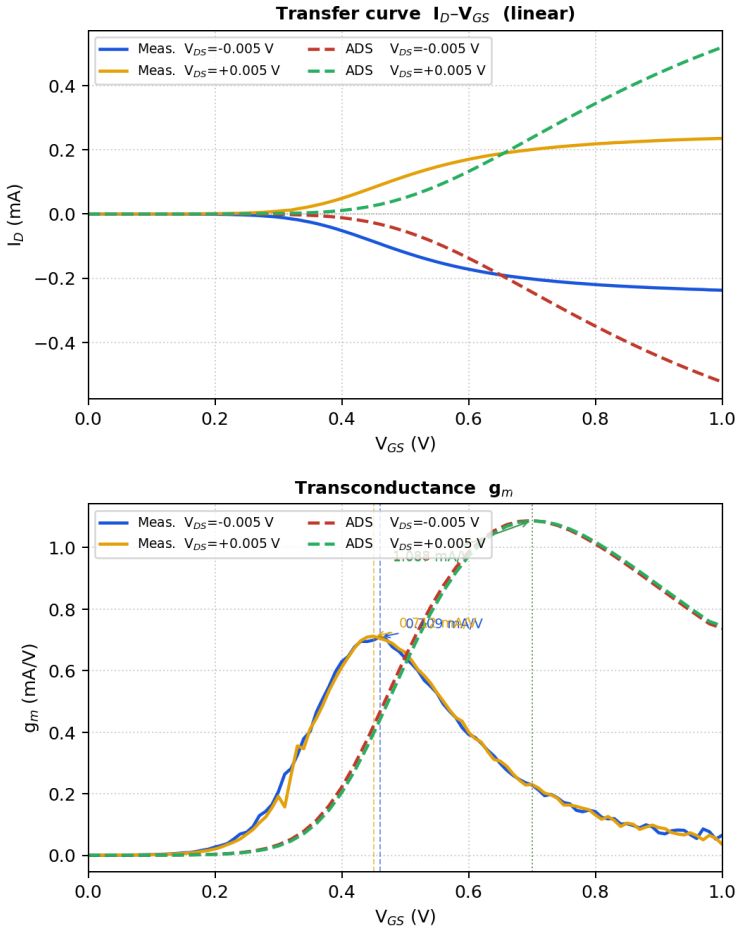

Fig. 3.2.1. I-V characteristics comparison between ADS and produced chip transistors

Big difference in this circuits are due to different characteristics of used transistors in fabricated chip and in simulated ADS design. Fabricated chip's transistor gate width is 10 µm, and gate length is 180 nm, which is less than transistor characteristics used in ADS model.

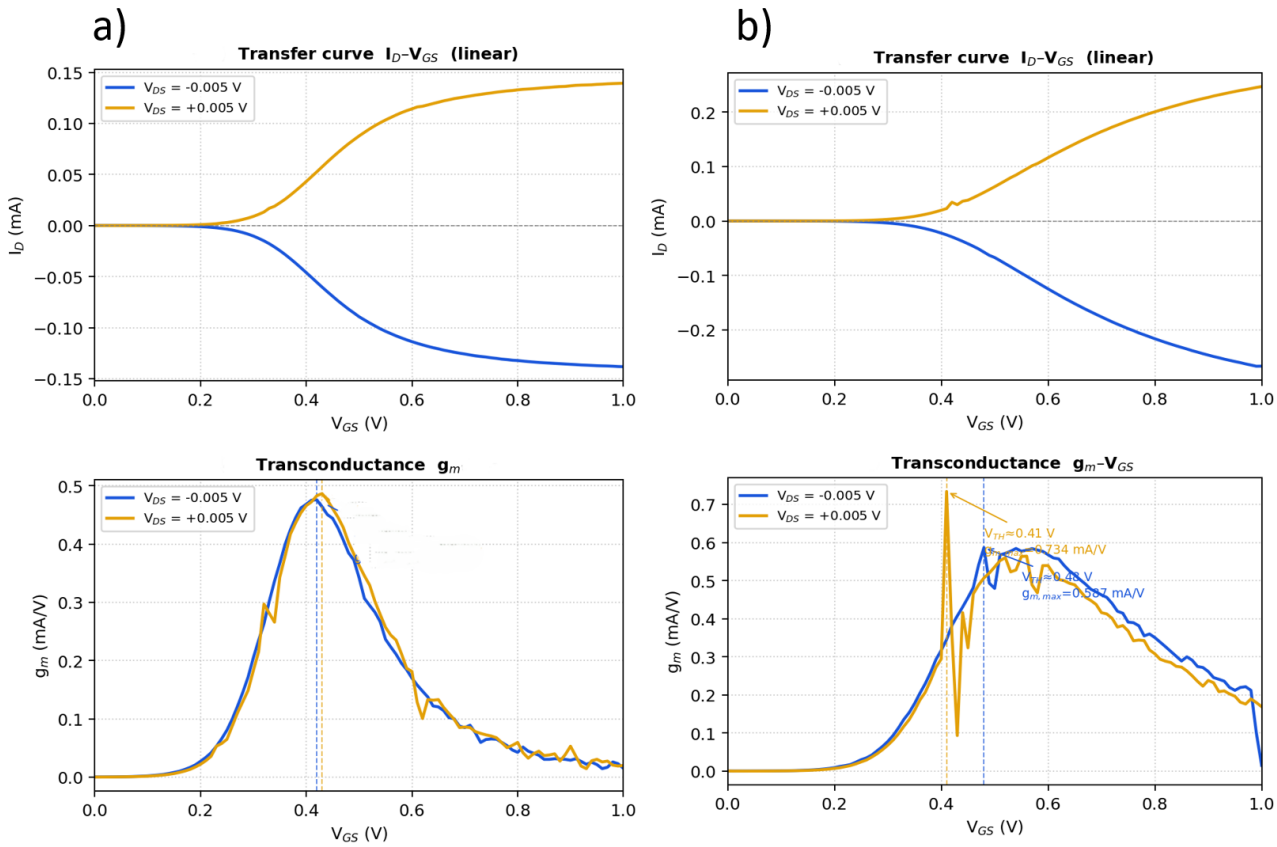

Fig. 3.2.2. I-V characteristics of transistors in a) tripler and b) amplifier in fabricated chip

It can be seen from fig. 2.3.2. that, optimal biasing of transistor is around 0.41 V and 0.43 V for tripler and amplifier respectively. There are 3 stages: Subthreshold region, linear region and saturation region. For the first region, transistor is off state, both transistors show low g_m here. The stage where peak g_m occurs is linear stage. It is 0.486 mA/V for tripler and 0.734 mA/V for amplifier. By the time V_{GS} hits V_{TH} + 0.30 V, g_m has already dropped from its high and it is in saturation region.

For tripler application transistor should biased at threshold (V_{TH}) or slightly below threshold to make nonlinearity (Class B/C). Because, linear transistor shouldn't be producing harmonics. For amplifier it should be biased at peak g_m, as in this region it has maximum gain.

Conclusions

To conclude, using CMOS technology, an entire D-band communication front-end was modelled in ADS. It consists of a bandpass filter, a Marchand balun, and power amplifier stages, and a frequency tripler and antenna. Moreover, layout design of elements have been done and compared with ideal elements characterization to study difference between them.

The simplified CMOS ADS Momentum substrate stack, consisting of a 150 μm absorbing silicon bulk and seven SiO_2 dielectric layers with $\varepsilon_r = 3.9$ has been constructed and used in EM simulation of layout elements.

The transistors are operating flawlessly, according to I-V testing conducted between prototype chip and ideal elements. The peak transconductance varied from 0.486 to 0.734 mA/V, the threshold voltage was between 0.41 and 0.46 V, and the gate leakage remained incredibly low at less than 1 nA across all tested devices. In the end, these measures demonstrate how highly consistent the production process was. Also, operation regions of transistors for tripler and amplifier applications has been determined.

Future work

For the future work, it is planned to do I-V and RF measurements using probe station for submitted and produced chip. And do simulations again to compare performances and find possible optimizations.

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Abstract

Higher frequency bands are the main matter of research due to the need for faster wireless communication systems. The D-band, which spans 110 to 170 GHz, has a large bandwidth that can accommodate the extremely high data rates required for upcoming 6G wireless networks. However, because components operate differently than at lower frequencies and typical simulation models do not necessarily match the behavior of produced chips, it is challenging to develop integrated circuits that function appropriately at these frequencies.

In the literature review, the components of this model are explained and the observed works are compared. In this thesis, the circuit for D-band frequency is prepared, the blocks in the system, i.e. Balun, Filter, tripler, passive elements, amplifier and antenna are characterized. The layout of the elements was prepared and compared with their ideal versions.

In this work, the difference between real and ideal models of the system has been studied and explained. A prototype chip has been fabricated and initial electrical measurements have been carried out. The measurements confirmed that all transistors are healthy, with gate leakage below 1 nA and consistent threshold voltages between 0.41 and 0.46 V. The literature review findings about optimal bias conditions for triplers and amplifiers are supported and have been discussed in the results of real chip transistors.

To conclude, the outcomes of this thesis include a collection of designed D-band frontend components with validated simulation methodology and a characterized understanding of the difference between simulation models and real devices.

Anotacija

Aukštesniojo dažnio juostos yra pagrindinis tyrimų objektas, kurį lemia spartesnių belaidžio ryšio sistemų poreikis. D juosta, apimanti 110–170 GHz dažnius, pasižymi didele pralaidumo juosta, galinčia užtikrinti itin didelį duomenų perdavimo greitį, reikalingą būsimiems 6G belaidžiams tinklams. Vis dėlto, kadangi komponentai veikia kitaip nei žemesniuose dažniuose, o įprasti modeliavimo modeliai nebūtinai atitinka pagamintų lustų elgseną, sukurti tinkamai šiuose dažniuose veikiančias integrines schemas yra iššūkis.

Literatūros apžvalgoje paaiškinami šio modelio komponentai ir palyginami nagrinėti darbai. Šiame darbe suprojektuota D juostos dažnio schema, charakterizuoti sistemos blokai: baluninis transformatorius (balunas), filtras, dažnio trigubintuvas, pasyvieji elementai, stiprintuvas ir antena. Paruošta elementų topologija (išdėstymas) ir palyginta su jų idealiosiomis versijomis.

Šiame darbe ištirtas ir paaiškintas skirtumas tarp realių ir idealių sistemos modelių. Buvo pagamintas lusto prototipas ir atlikti pirminiai elektriniai matavimai. Matavimai patvirtino, kad visi tranzistoriai yra veikiantys: užtūros nuotėkio srovė nesiekia 1 nA, o slenkstinė įtampa yra stabili ir svyruoja tarp 0,41 ir 0,46 V. Literatūros apžvalgos įžvalgos apie optimalias trigubintuvų ir stiprintuvų priešįtampio sąlygas yra pagrįstos ir aptartos remiantis realaus lusto tranzistorių rezultatais.

Apibendrinant, šio darbo rezultatai apima suprojektuotų D juostos priekinės dalies (angl. *frontend*) komponentų rinkinį su patvirtinta modeliavimo metodika bei charakterizuotą supratimą apie skirtumus tarp modeliavimo modelių ir realių įrenginių.