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Integration of the upgraded CMS data readout system for LHC Phase-2

Rocco Ardino[a], **Miguel Bacharov Durasov**[a], **Ulf Behrens**[b], **Andrea Bocci**[a], **James Branson**[c], **Philipp Maximilian Brummer**[a], **Sergio Cittolin**[c], **Georgiana-Lavinia Darlea**[d], **Christian Deldicque**[a], **Marc Dobson**[a], **Antonin Dvorak**[a], **Dominique Gigi**[a], **Frank Glege**[a], **Guillelmo Gomez-Ceballos**[d], **Patrycja Gorniak**[a], **Jeroen Hegeman**[a], **Thomas Owen James**[a], **Wassef Karimeh**[a], **Wei Li**[b], **Constantinos Loizides**[b], **Kenneth Long**[d], **Frans Meijers**[a], **Emilio Meschi**[a], **Srećko Morović**[c], **Luciano Orsini**[a], **Christoph Paus**[d], **Andrea Petrucci**[c], **Marco Pieri**[c], **Dinyar Sebastian Rabady**[a], **Attila Racz**[a], **Theodoros Rizopoulos**[a], **Hannes Sakulin**[a], **Christoph Schwick**[a], **Dainius Simelevicius**[a,e], **Polyneikis Tzanis**[a,*], **Cristina Vazquez Velez**[a] and **Petr Zejdl**[a]

[a] *CERN, Geneva, Switzerland*
[b] *Rice University, Houston, Texas, U.S.A.*
[c] *University of California, San Diego, San Diego, California, U.S.A.*
[d] *Massachusetts Institute of Technology, Cambridge, Massachusetts, U.S.A.*
[e] *Vilnius University, Vilnius, Lithuania*

E-mail: polyneikis.tzanis@cern.ch

Abstract: The CMS Phase-2 upgrade of the CMS Data Acquisition (DAQ) system is based on the DAQ and Timing Hub (DTH) board. The DTH serves as an interface, connecting sub-detector front-end electronics to the DAQ, as well as timing and trigger control and distribution system. This work focuses on the DAQ functionality of the DTH, detailing the current status of the project, including the DAQ firmware and control software. First integration with Phase-2 sub-systems and future plans are presented.

Keywords: Control and monitor systems online; Data acquisition circuits; Modular electronics; Software architectures (event data models, frameworks and databases)

*Corresponding author.

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1 The CMS DAQ Phase-2 architecture

The Compact Muon Solenoid (CMS) [1, 2] experiment at the CERN Large Hadron Collider (LHC) is preparing for the High-Luminosity LHC (HL-LHC) era, in order to face the increase of the instantaneous luminosity by an order of magnitude. To handle the increased data volume, the DAQ and the Trigger Control and Distribution System (TCDS) are being upgraded to sustain a Level-1 trigger rate of 750 kHz and a 30-fold increase in data throughput compared to Run 3.

As shown in figure 1, the planned Phase-2 DAQ architecture consists of new detector back-end electronics providing timing and data processing through a high-performance network. The custom hardware for the DAQ is based on two custom Advanced Telecommunications Computing Architecture (ATCA) boards [3]: the DTH-400 and the DAQ-800, which aggregate, buffer, and distribute detector data before sending them to the central event builder farm. Sub-detectors transmit data over custom high-speed optical links ("SlinkRocket":25 Gbps [4]) to the DTH and DAQ boards, where data are

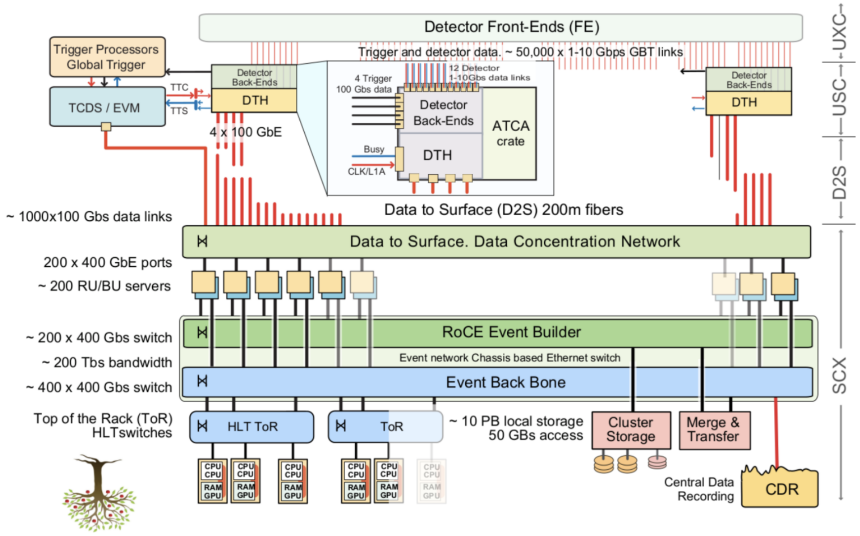

Figure 1. Overview of the CMS Phase-2 DAQ and TCDS architecture. The upgraded system integrates detector back-end electronics, timing distribution, and data aggregation through high-performance network infrastructure.

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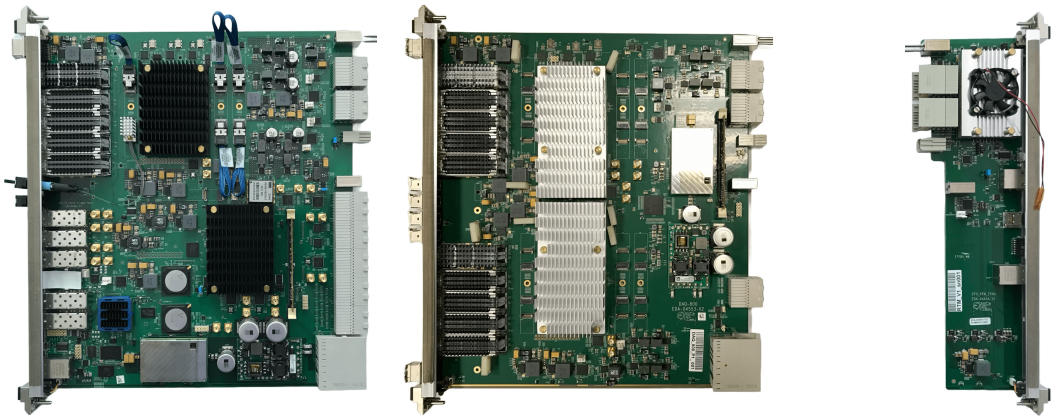
aggregated, buffered using High Bandwidth Memory (HBM), and transmitted over standard 100 Gbps TCP/IP (adapted to higher bandwidth [5]) links, via the event builder [6, 7] to the High-Level Trigger (HLT) systems. A software-based orchestration layer [8, 9] based on Kubernetes, manages control and monitoring across the distributed DAQ infrastructure.

2 Hardware

Two custom ATCA boards [10, 11] with the accompanying Rear Transition Module (RTM) board, have been developed to serve the full range of CMS Phase-2 DAQ requirements:

- *DTH-400*. The DTH-400, as shown in figure 2(a), is an ATCA hub-card equipped with dual-FPGA board featuring two AMD (Xilinx) Virtex UltraScale+ VU35P FPGAs, each containing 8 GB of HBM. One FPGA implements the TCDS functionalities (trigger control, timing, and synchronization) while the second performs high-speed DAQ data aggregation. Data from up to six 4-channel Samtec Firefly optical engines (24 × 25 Gbps) are aggregated to a total throughput of 400 Gbps and transmitted as multiple TCP/IP streams over 100 Gbps via QSFP28 transceivers. The HBM implements large TCP/IP socket buffers, maintaining high-throughput network operation in the presence of fluctuations of the receiving end.
- *DAQ-800*. The DAQ-800 board, as shown in figure 2(b), is an ATCA leaf-card which is used when data throughput over 400 Gbps is needed. It integrates two DAQ FPGA units equivalent to those of the DTH-400, offering an aggregate throughput of 800 Gbps. It is used by high-bandwidth sub-detectors, TCDS Captain [12] and the CMS Level-1 scouting readout [13].
- *RTM*. The RTM, as shown in figure 2(c), provides control and monitoring capabilities for both DTH-400 and DAQ-800 boards. It is based on an AMD Kria K26 SoM, integrating a Zynq UltraScale+ MPSoC. The 2 FPGAs are connected to the MPSoC via Advanced eXtensible Interface (AXI) Chip2Chip buses. The programmable logic is mapped to the processing system via the AXI bus, accessible in Linux via device tree and Userspace I/O. Network boot is provided via standard services (DHCP, TFTP, NFS, NTP). The modular architecture allows for an upgrade of the processing node without changing the main ATCA boards.

The pre-series boards [12] have been validated successfully, and production has been launched.



(a) DTH-400 board (b) DAQ-800 board (c) RTM board

Figure 2. Photographs of the three main boards: (a) DTH-400, (b) DAQ-800, and (c) RTM.

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3 Data readout firmware

The DTH DAQ firmware [12], as shown in figure 3, implements the high-speed data path required for Phase-2 readout operations. It supports up to 24 SlinkRocket inputs received via Samtec Firefly optical links, interfacing the sub-detector back-end electronics with the DAQ FPGA. The TCDS FPGA distributes timing, trigger, and fast control signals, ensuring deterministic event-level synchronization across all sub-detectors. The DTH aggregates data fragments for collisions occuring in one LHC orbit separately for each SlinkRocket input stream, while the integrated HBM provides high-throughput buffering for TCP/IP [5] transmission. A firmware TCP/IP engine manages data encapsulation and Stream Distribution Box which provides configurable routing of SlinkRocket back-end links to the 100 Gbps TCP/IP output links.

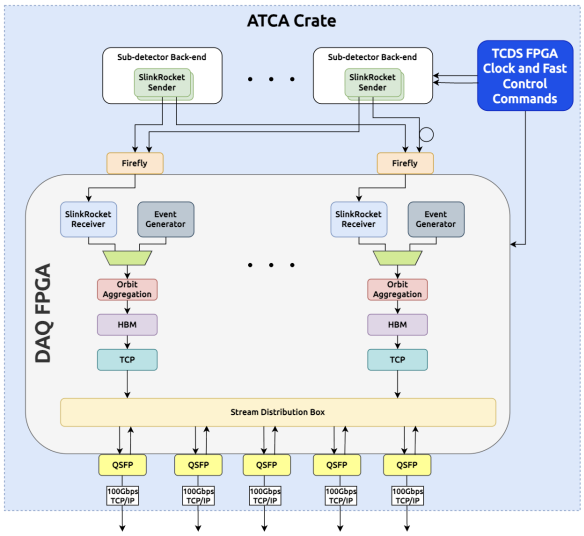

Figure 3. Block diagram of the DTH DAQ data readout firmware. The design implements SlinkRocket input, orbit aggregation, high-speed buffering using HBM, and 100 Gbps TCP/IP output via the Stream Distribution Box.

4 Control software

The control software stack, as illustrated in figure 4, is designed for modularity, efficiency, and seamless integration with the CMS online infrastructure. It is developed primarily in C++ based on the CMS online software XDAQ [8, 9] framework, optimized for execution in embedded environments with limited computational resources. Python bindings are provided for testing and debugging. Hardware access is achieved through a Linux Userspace I/O driver, which maps internal registers of programmable logic of the two main FPGAs to user space via AXI Chip2Chip buses. The control software architecture follows a layered and modular design for the various components. A single controller process hosts the Representational State Transfer (REST) API, a common web service interface, and the Finite State Machine (FSM) engine, while the monitoring publishes metrics to an external Message Queuing Telemetry Transport (MQTT) broker, a lightweight publish/subscribe system. Control and configuration commands are exposed through a REST API, providing endpoints for device setup and FSM transitions. Responses are returned synchronously via structured JSON payloads. Monitoring data are streamed

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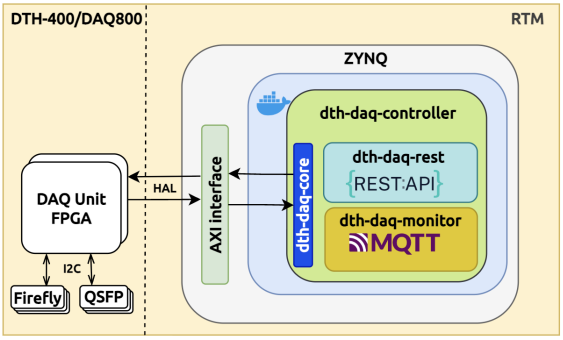

Figure 4. Architecture of the DTH DAQ control software. The modular C++/Python stack integrates RESTful control interfaces, MQTT-based monitoring, and containerized deployment.

asynchronously using MQTT topics with configurable publish rates. Redundancy is supported by providing REST-based monitoring as a fallback mechanism. To ensure maintainability and portability, the system supports structured text formats (JSON/YAML) configuration profiles with hierarchical parameter overrides and selective hot-reloading of components. The entire software stack is built with automation practices combining development and operations (DevOps) based on GitLab Continuous Integration and Deployment (CI/CD) pipelines. The automated workflow covers building, unit testing, packaging into Linux binary packages (RPMs), and container image generation. The container images can be deployed as standalone services or via deployment/orchestration tools based on Helm charts within a Kubernetes-managed environment [9]. Documentation and tools accompany the system to facilitate maintenance and troubleshooting. This architecture ensures a robust, maintainable, and extensible control system capable of supporting the demands at the HL-LHC era.

5 Kit distribution

DTH integration kits have been distributed to CMS sub-detectors to facilitate early-stage firmware and software integration with the central DAQ system. Each kit comprises a DTH-400 board, an RTM, and a complete suite of firmware, control software, and containerized network services. Continuous technical support is provided to ensure efficient integration, debugging, and validation of sub-detector back-end electronics, enabling a smooth transition toward full system commissioning within the Phase-2 DAQ architecture.

6 Demonstrator

A demonstrator "DAQ column", as shown in figure 5, integrating Phase-2 hardware and several software components, has been developed to test all Phase-2 developments in a vertical slice. This demonstrator provides a complete end-to-end validation platform for the Phase-2 readout chain, enabling functional testing of firmware, software, and data flow from detector emulators to the CMS Offline Software (CMSSW) based event processing framework of the HLT. The setup replicates realistic operational conditions, featuring network booting, containerized services, and orchestration through the Run Control Software System (RCSS) [14] via Kubernetes. It also includes DAQ receiver applications and CMS input plugins, ensuring compatibility and seamless integration with the central online system.

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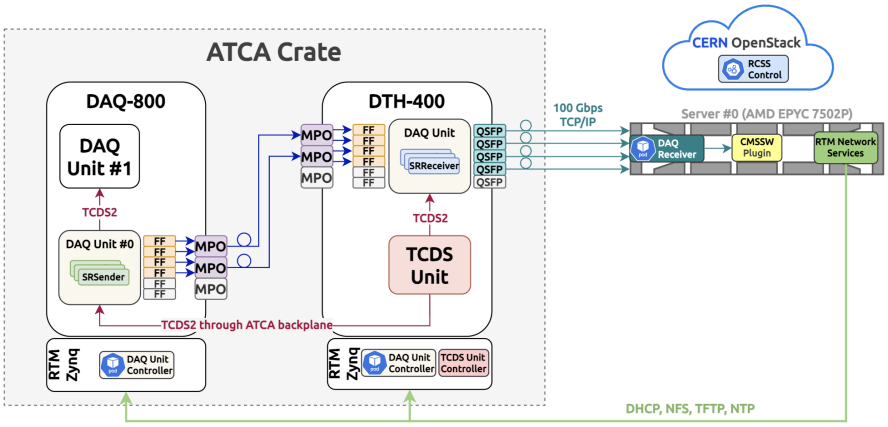

Figure 5. The Phase-2 DAQ demonstrator setup, featuring DTH-400 and DAQ-800 boards, RTMs, and control software. The system enables full end-to-end validation of firmware, software, and data flow from sub-detector emulators to CMSSW-based event processing.

7 Integration facility

An Electronics Integration Facility is currently being setup for large-scale integration and testing of CMS Phase-2 sub-detector systems with the central DAQ and TCDS infrastructure. The facility hosts multiple ATCA crates instrumented with DTH-400 board, interconnected through a common network switch featuring common 10 and 100 GbE. In addition, a dedicated computing infrastructure is available for sub-detector teams, providing a containerized environment to run their software and monitoring applications. This setup enables concurrent integration of multiple sub-detectors within a unified environment, allowing comprehensive validation of firmware, control software, timing distribution, and data flow across the entire DAQ chain. It serves as a central platform for debugging and pre-commissioning of sub-detector back-end electronics prior to installation in the CMS experimental cavern. As the Phase-2 upgrade advances, the facility continues to expand, integrating additional sub-detectors and evolving toward a multi-crate, system-level demonstrator of the complete CMS Phase-2 DAQ architecture. Ultimately, it will transition into the final CMS online system, fully orchestrated by Kubernetes and mirroring the operational environment to be deployed during HL-LHC data taking.

8 Summary

The CMS Phase-2 DAQ upgrade is evolving rapidly across hardware and software components. The DTH-400 and DAQ-800 boards have been validated, with production underway. Firmware and control software development continue to evolve, enabling stable, scalable data readout. DTH kits have been successfully distributed to sub-detectors, supporting smooth integration and system-level validation. The Integration Facility at CERN provides the platform for multiple sub-detector commissioning and performance testing. Together, these developments allow the CMS DAQ project to evaluate its components for handling the high-rate data acquisition required by the HL-LHC.

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